Warsaw University of Technology

FACULTY OF
ELECTRONICS AND INFORMATION TECHNOLOGY

Instytut Systemów Elektronicznych

Bachelor's diploma thesis

in the field of study Electronics
and specialisation Elektronika i inżynieria komputerowa

Microwave synthesizer for driving ion traps in quantum computing

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Warsaw 2019

Abstract

Microwave synthesizer for driving ion traps in quantum computing

The following bachelor thesis describes the design of the microwave synthesizer - an EEM peripheral extension module for Sinara ecosystem developed for applications in trapped-ion experiments in the field of quantum physics. The device is based on four PLL/VCO synthesizers: ADF5356 from Analog Devices.

The subsequent chapters present the individual stages of the project implementation: a selection of components, PCB design, verification, and prototype testing. At the same time, key information about the designed device was also presented.

Keywords:

Synthesizer, high frequency, PCB, Altium Designer, ion traps, ARTIQ, Sinara.

Streszczenie

Syntezer wielkich częstotliwości do pułapek jonowych w komputerze kwantowym

Poniższa praca zawiera opis projektu syntezera mikrofalowego - modułu EEM będącego rozszerzeniem peryferiów dla ekosystemu Sinara, do zastosowań w eksperymentach z dziedziny fizyki kwantowej. Urządzenie oparte jest na czterech syntezerach PLL/VCO: ADF5356 firmy Analog Devices.

W kolejnych rozdziałach przedstawiono poszczególne etapy realizacji projektu: dobór komponentów, projekt PCB, weryfikację oraz testy prototypu. Równolegle przedstawione zostały także kluczowe informacje dotyczące projektowanego urządzenia.

Słowa kluczowe:

Syntezer, wielkie częstotliwości, PCB, Altium Designer, pułapki jonowe, ARTIQ, Sinara.

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Contents

1. Introduction

Electronic equipment used in many trapped-ion and other quantum physics experiments is expected to meet ever-increasing performance requirements. This usually involves dedicated solutions, which are often hastily designed with the only consideration being the current project criteria. Additionally, the effort spent on the design of such equipment is often duplicated across different laboratories. As such, those systems can be difficult to use and maintain, and their performance or features may not be sufficient for other, future projects. Sinara - an open-source hardware ecosystem, part of which is the presented project, aims to alleviate this problem[1].

This thesis describes the design of an instrument intended for use in various quantum physics experiments, mainly for use with trapped-ion research. The following chapters discuss the design process: starting from the project specification and selection of components, through the circuit diagram and the printed circuit board, project verification, to the tests of the prototype. The full extent of the project files can be found on the project repository[1]. Schematic drawings, PCB masks, project verification simulations, and CPLD code have been included in the appendices at the end of this thesis.

1.1 Ion traps

The basic information unit used in quantum computation - a qubit - can be implemented as an ion or other charged particle: cooled, confined and isolated[2] inside an ion trap. As an example: one of the most common traps used in experiments is a Paul trap (also known as quadrupole trap), based on a set of two opposing conical electrodes and a ring electrode halfway between the other two. A combination of oscillating and static electric field with right parameters applied to the electrodes forms the desired potential and suspends individual particles in the center of the trap[2].

[1] https://github.com/sinara-hw/mirny/

[2] Due to low energies involved in the experiments, heat (random kinetic energy), electromagnetic fluctuations or external mechanical forces can corrupt stored information.

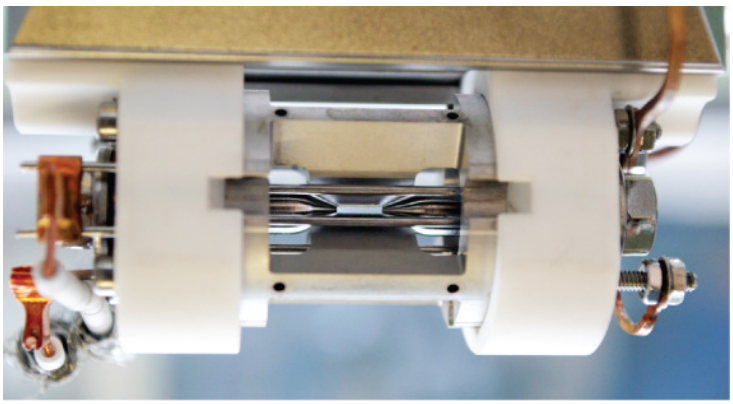


Figure 1.1: Quadrupole ion trap

Source: IQOQI Innsbruck, https://quantumoptics.at/images/qsim/iqoqi_trap.jpg

Information stored in the captured qubits is usually manipulated via laser beams[3]. And thus, an optical control system is needed. Most commonly electro-optic or acousto-optic modulators are used for this task, providing beam control needed for the experiments.

1.2 Purpose and scope of work

The goal of this thesis was to design, manufacture and test a microwave synthesizer module named *Mirny*, intended for use in trapped-ion experiments in the field of quantum physics. The range of applications includes control of acousto-optic and electro-optic modulators and generation of low-noise microwave frequencies for other equipment.

[3] Tuned laser beams (frequency and power-wise) allow for energy manipulation of the particle, as absorption and emission of a photon by an ion is accompanied by momentum transfer[2].

2. Design

2.1 Specification

The PLL/VCO-based microwave frequency synthesizer designed over the course of this thesis aims to be a low-cost, easy to use and well-tested piece of equipment, capable of being used in multiple science experiments and with the possibility of future expansion. Based on the possible future applications, as the synthesizer is intended mainly for tasks such as driving AOMs/EOMs[1], the requirements for the finished device are:

- compatibility with Sinara ecosystem[1][3],
- EEM form factor[2],
- four independent channels,
- resolution of few kHz or better,
- control over SPI and few TTL signals,
- output bandwidth of approximately 40 MHz to 4 GHz,
- low phase noise,
- internal frequency reference with a precision few parts per milion,
- user mountable filters (both comercially available and discrete),
- optional frequency multipliers (2x, 3x or 4x) allowing higher output bandwidth,
- analog front-end consisting of:
  - filter,
  - amplifier,
  - adjustable attenuator,
  - RF switch.

[1] Acousto-optical modulators and electro-optical modulators

[2] EEM, 'Eurocard Extension Module' - peripheral extension card standard adopted for Sinara devices. Compatible with standard 3U 19-inch racks. Card width can be either 4HP or 8HP.

2.2 General concept

The following chapter describes the construction concept of the microwave synthesizer module. The device has been divided into basic functional blocks (as shown in fig. 2.1), and the functionality each segment has been discussed.

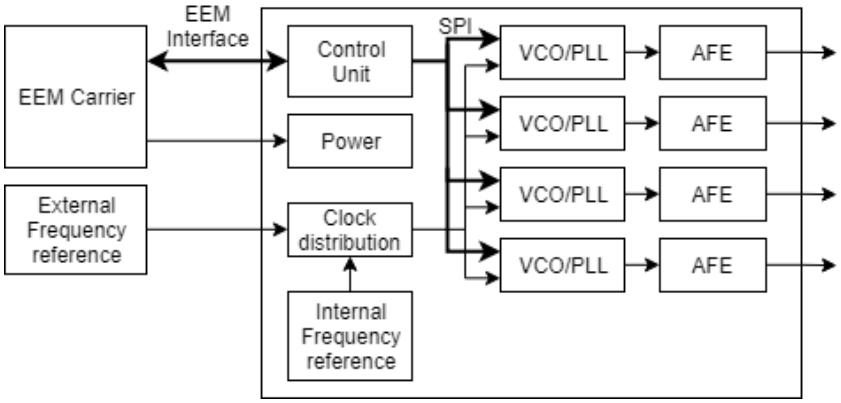


Figure 2.1: System block diagram

2.2.1 Clock distribution

This unit consists of an internal frequency reference and a switch, that allows for choosing between the external and internal sources. The switch should incorporate or be followed by a buffer that provides a reference signal of appropriate power to the VCO/PLL unit.

2.2.2 VCO/PLL and AFE

Both of the mentioned design segments form a single analog channel of the module: a frequency synthesizer followed by the desired analog path components. As such, they are the core of the design and meet most of the design specification requirements.

2.2.3 Control Unit

The control unit acts as a communication bridge between the EEM interface and other design segments, such as the synthesizer chips. This also includes the devices connected via I2C, such as the identification EEprom and the thermal sensor.

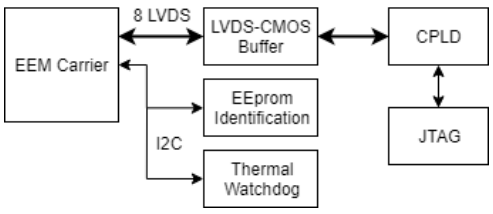


Figure 2.2: Control Unit diagram

2.3 Component selection

Prior to the development of the circuit board, it was necessary to select all main components together with their respective values. The key components which will determine most of the performance and functionality are the frequency synthesizer and the devices used in the analog path. Thus it is important to pay special care in comparing available solutions and choosing the most suitable ones. The main criteria were the use of devices already proven in previous projects and the minimization of output phase noise. The schematic prints with selected components have been included in appendix A.

Frequency synthesizer

The core component of this module, which will define most of the functionality and performance is the frequency synthesizer chip. Two families of PLL based synthesizers with integrated voltage tuned oscillators were considered for generating the output signal: ADF435x/ ADF535x[4][5] and HMC833[6] from Analog Devices (comparison is presented in table 2.1).

Table 2.1: Available synthesizer chips comparison

	ADF5356	ADF4355	HMC833LP6GE
output frequency range	53,125 - 13600 MHz	54 - 4400 MHz	25 - 6000 MHz
frequency resolution	0,1 mHz	0,1 mHz	3 Hz
RMS Jitter	97 fs	150 fs	180 fs
normalized VCO noise 1/f[1]	-115 dBc/Hz	-116 dBc/Hz	-110 dBc/Hz
output power range	-4 do 5 dBm	-4 do 5 dBm	0 do 9 dBm
output power resolution	3 dBm	3 dBm	3 dBm
required supply voltages	3,3 V and 5 V	3,3 V and 5 V	3,3 V and 5 V
current consumption[2]	176,4 mA and 78 mA	170,8 mA and 78 mA	57 mA and 193 mA
power consumption	0,972 W	0,954 W	1,153 W
case size	25 mm^2	25 mm^2	36 mm^2
price per unit[3]	277,39 PLN	116,68 PLN	79,66 PLN

[1] Includes noise 1/f (flicker) and normalized PLL noise level,

[2] Respectively for 3,3V and 5V supply,

[3] Price for detail order from mouser, as of 17 November 2018.

Better noise performance, wide frequency range and compatibility with other synthesizer chips from Analog Devices, made ADF5356 an easy choice. Product families ADF435x and ADF535x are fully pin-compatible and cover an output frequency range of 54 MHz to 13.6 GHz. This allows for the assembly of multiple versions of Mirny synthesizer if higher output frequencies are not needed and the cost is an issue. At the same time, if the already assembled device does not cover the required frequency range, it could be easily upgraded by changing the synthesizer chips. This also deems external frequency multipliers unnecessary, as the synthesizer chip family covers the specified output bandwidth due to an integrated frequency doubler.

PCB Substrate selection

The selected synthesizers allow the generation of output frequencies up to 13.6 GHz. Unfortunately, the standard FR4 substrate is characterized by significant losses at higher frequencies, which makes it impractical to use it above 4-6 GHz[7]. Initially, analog front-end was planned in the form of small castellated[3] modules on Rogers substrate, which would be soldered onto the main FR4 PCB. Such a solution would cover a wide frequency range, be much cheaper than manufacturing the entire board on Rogers substrate and would enable the design of custom versions of analog front-end or its subsequent modification.

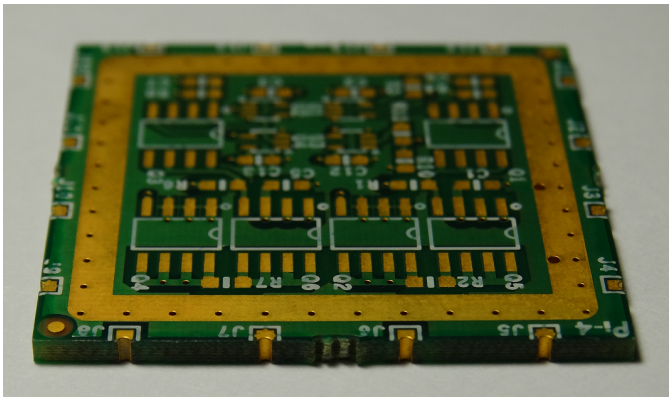


Figure 2.3: Example of a castellated PCB module

Source: http://www.saturnpcb.com/pcb_manufacturing_services/

Selected synthesizer chips (eg ADF5356) have two signal outputs: main output connected to a VCO divider and a complementary output connected to a frequency doubler bypassing the VCO divider. Therefore, the divided outputs of each synthesizer can be routed to the front panel connectors, and the FR4 substrate can be used for the entirety of the PCB. Such configuration, however, limits the bandwidth by FR4 performance - up to approximately 4-6 GHz. In order to generate higher frequencies, the multiplied outputs were routed to SMP connectors located near the synthesizer chips, directly on the PCB. Due to the short distance between the connectors and the synthesizer chips, the substrate losses

[3] PCB with metalization on board edge

should not significantly attenuate the signal. To use doubled outputs, an additional module with 4 SMA sockets should be installed next to the Mirny module. Each front panel connector would be internally connected via a short cable[4] directly to the corresponding SMP connector (fig. 2.4a). Such a solution, however, does not offer any functionality of the basic analog path: filtration, amplitude regulation and signal switching, and directly outputs the doubled frequency generated by the VCO. To enable the future design of an optional AFE board, some CPLD control signals and power rails have been routed to a dedicated board to board connector. The predicted current consumption of optional AFE board has been included in the power consumption calculation and the construction of the power supply.

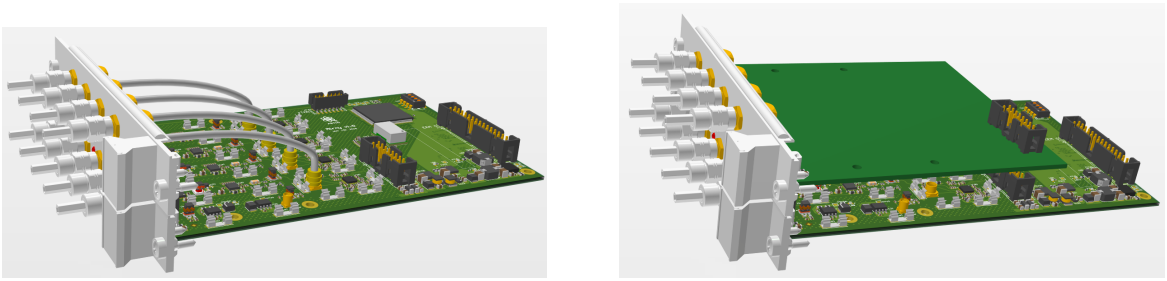


Figure 2.4: High frequency RF output and AFE module

Analog front end

As the selected FR4 substrate already limits the output bandwidth, an analog path with a higher bandwidth would not benefit the design. Thus, components that work in a range limited to approximately 4-6 GHz and have already been used in other projects have been selected for the analog front-end implementation[5].

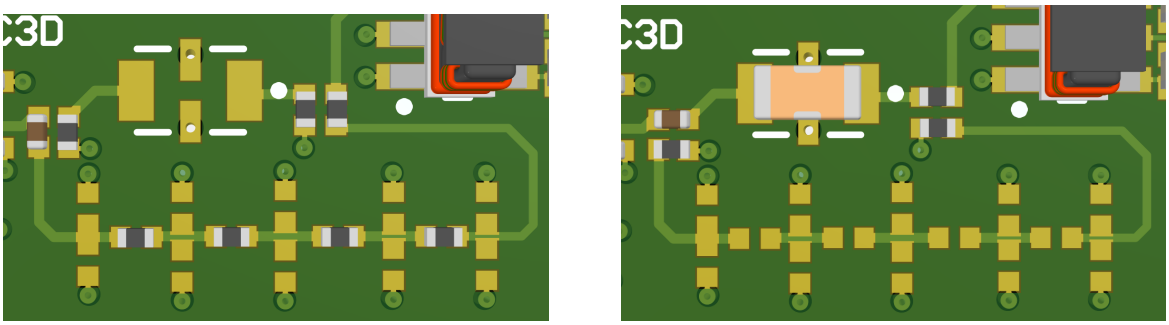
The first component on the signal path is a *TCM2-43X+* balun transformer (TR1), which connects the symmetrical output of the synthesizers to the single-ended path. Its role is also to match the 100 Ω impedance of the synthesizer output to the 50 Ω AFE components.

The signal path is then split by a set of jumpers: R47/R49 and R48/C49 (fig. 2.5, fig. 2.6), transmitting the signal either through a *FV1206* MiniCircuits filter or through a discrete-element filter designed by the user (with empty solder pads exposed for its implementation). This allows for usage of either custom designed or commercially available filters, or as it is in the default case: for omitting the filter (fig. 2.6).

The next components are the *HMC542BLP4E* attenuator (adjustable in the range of 0-31.5 dBm with 0.5 dBm steps) and the *ERA-4XSM+* amplifier with a gain of +13 dBm in the 0-4 GHz band. This combination allows for amplitude regulation in a range, that in most intended cases will not require additional, external attenuators or amplifiers.

[4] Patch cord - a short cable assembly fitted with connectors on both ends, also known as a 'pigtail'

[5] AFE components were previously used in similar EEM module - *Urukul* - `https://github.com/sinara-hw/Urukul`



(a) Discrete filter - default assembly

(b) FV1206 filter - optional assembly

Figure 2.5: Possible filter configurations

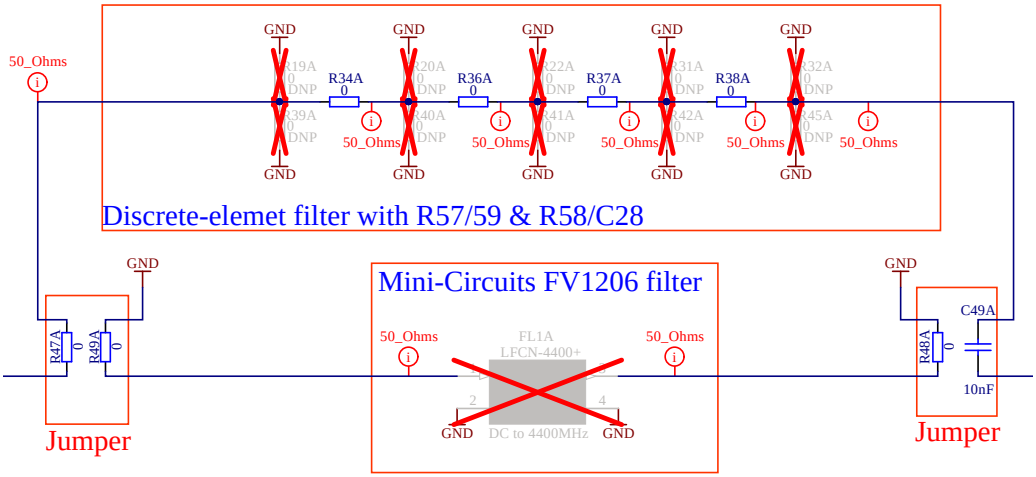


Figure 2.6: Schematic fragment (page 5) - AFE filters

With the maximum output power of the synthesizer chips (5 dBm), power at the amplifier input could cause compression [8] and lead to signal distortion. However, passing the signal through the attenuator first would reduce signal power by the insertion loss of HMC542BLP4E, and would not require additional attenuation before the amplifier.

Amplifier output power with 1 dB compression at the frequency of 1 GHz:

$$P_{1dB} = 15\ dBm$$

Thus, the maximal amplifier input power without signal compression:

$$P_{in\_1dB} = P_{1dB} + 1\ dB - G(1\ GHz)$$

$$P_{in\_1dB} = 15\ dBm + 1\ dB - 13\ dB$$

$$P_{in\_1dB} = 3\ dBm$$

Maximal synthesizer output power:

$$P_{IC9max} = 5\ dBm$$

Maximal power at the amplifier input:

$$P_{in\_IC2} = P_{IC9max} - P_{IL\_TR1} - P_{IL\_FL1} - P_{IL\_IC3} - P_{IL\_IC2}$$
$$P_{in\_IC2} = 5\ dBm - 0,5\ dB - 0,5\ dB - 1,5\ dB = 2,5\ dBm$$

Where $P_{IL\_TR1},\ P_{IL\_FL1},\ P_{IL\_IC3},\ P_{IL\_IC2}$ are the insertion losses of the components (balun, filter, attenuator and the amplifier). Which proves that such configuration does not require additional attenuation, as $P_{in\_IC2} < P_{in\_1dB}$.

The last component is the SPDT[6] switch - *HMC349ALP4CE*. Direct control via the EEM connector and equalizing trace lengths on the PCB, which ensures equal propagation time, allows benefiting from high timing resolution of the EEM interface. This functionality may be required in some of the intended use-cases, such as driving electro-optical modulators where precisely controlled RF bursts are needed.

Selected components limit output bandwidth of base board to 53-4000 MHz. Additionally, the frequency range of outputs for additional AFE is: 6.8-13.6 GHz with ADF5355/ADF5356 chips and 54-6800 MHz with ADF4355/ADF4356 chips. This means, that with the ADF5355/ADF5356 configuration, there is a 4-6.8 GHz gap in the output bandwidth: base board works in the 54-4000 MHz range, and the optional outputs cover 6.8-13.6 GHz. Thus, the generation of frequencies in the 4-6.8 GHz range requires either: using ADF4355/ADF4356 synthesizer chips which would limit frequency range to 6.8 GHz, implementing a frequency divider on the optional AFE or redesigning the front-end, so that its components would cover frequencies up to 6.8 GHz (which would be pushing the capabilities of FR4 substrate).

[6] 'Single pole, double throw' - bistable switch with one input and two possible outputs.

Optional analog front-end

Generation of frequencies highier than 4 GHz (due to limits mentioned earlier) without losing the functionality of base analog path, requires an optional analog front-end PCB. Design of such board is not covered by the scope of this work, but it should be considered during component layout and power supply design.

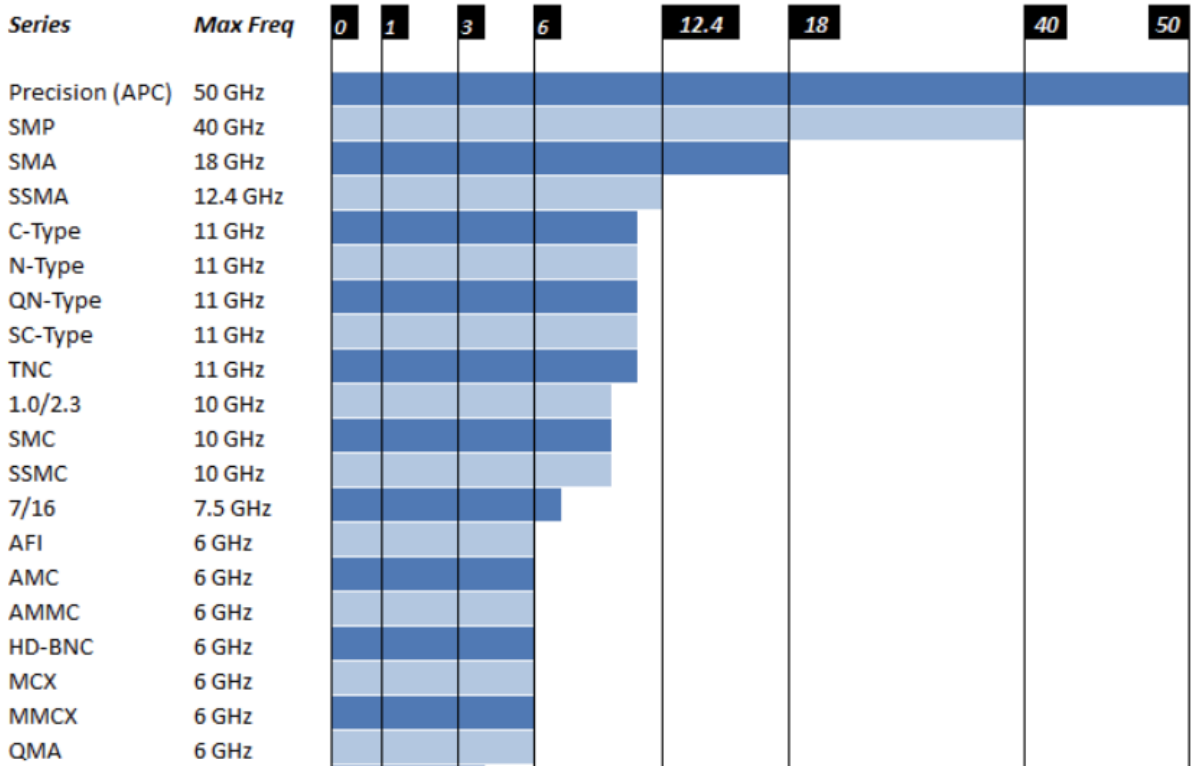


Figure 2.7: Maximal frequency of operation vs connector type

Source: https://www.amphenolrf.com/frequency-range-chart/

Control signals and supply voltages are supplied via a single IDC connector. The optional AFE board should be designed in the form of an adjacent EEM card connected to the base board using an IDC cable, or by using a standard 2.54 mm header soldered instead of one of the IDC connectors. To reduce confusion and to protect the device against a connection of the incorrect IDC cable, eg against connection of the 30-pin EEM connector (J1) cable, a connector with a fewer number of leads was chosen.

Depending on the synthesizer chip used, the frequency of the complementary output could range up to 13.6 GHz. As such, the performance of the MMCX connectors preferred for this use would not be sufficient, so to ensure adequate frequency range the SMP connectors have been chosen. Small size and availability of various SMP-SMA and SMP-SMP cable assemblies allow for easy connection of either directly to the front panel or to the adjacent optional AFE board.

Table 2.2: Example components for optional AFE

Component	Description	Required supply voltages[1]
EHC-24L+	amplifier, +13 dBm, DC-20 GHz	+5 V/ 19,1 mA
ADRF5720	attenuator, 0-31.5 dBm, 9 kHz-40 GHz	+3.3 V/ 117 µA, -3,3 V/ 117 µA
MASW-008322-TR1000	switch, SPDT, DC-20 GHz	-5 V/ 100 µA

[1] Additionally, control circuits would be supplied by +3.3 V rail

In order to determine the required supply voltages, current consumption and the required number of control signals, an exemplary set of analog path elements was selected. Based on the component selection listed in table 2.2, supply rails: +5.5 V, +3.3 V and +12 V (for an inverting converter) would be enough for proper operation. One could suspect, however, that it would be desirable to include more powerful amplifiers on the optional AFE board. As such, +7.5V rail was also routed to the connector. The coverage of multiple, evenly spaced voltages should reduce the number of switching converters to the inverting converter, which will significantly minimize generated noise and cost.

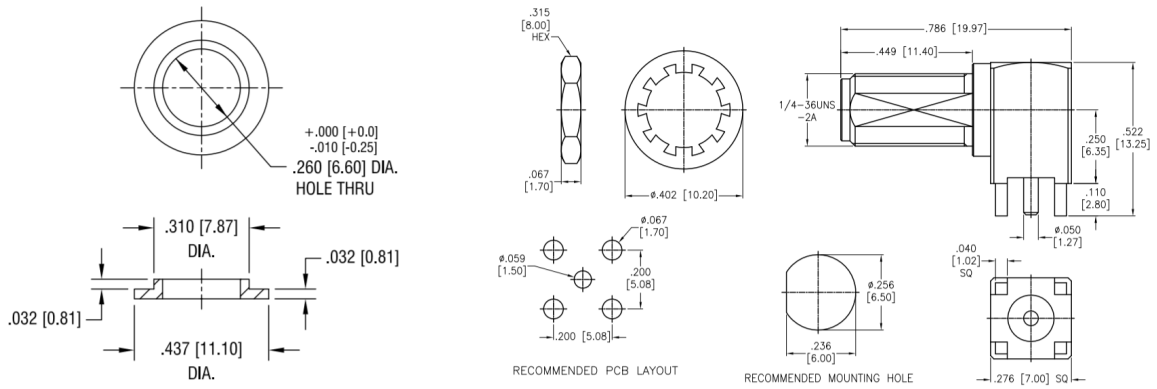
To provide control and communication with the additional board, 8 CPLD IO[7] lines were assigned: 4 lines dedicated for SPI communication (SCK, MISO, MOSI, CSN) and 4 for output switches control. To keep consistency with the base synthesizer, the IO lines between the CPLD (IC10) and AFE connector (J10) have been length-matched. Additionally, the I2C bus routed to the connector for identification of the future AFE card or the measurement of its temperature.

[7] 'input-output'

Front panel

One of the design specification requirements was a format of a rack-mounted EEM card. Due to relatively small power consumption and low profile elements used in the design, a 3U4HP[8] front panel size has been chosen.

The next step was the selection and placement of front panel components so that they are optimally distributed and that access to none of the connectors is restricted. After a review of the available SMA connectors in terms of their size and maximum operating frequency, the *RF249BT0050GHDW* connector from *Adam Tech* was selected. The frequency range of up to 6 GHz will be sufficient for the base version of the synthesizer.



(a) Insulating washer - Keystone 7687

(b) SMA connector - RF249BT0050GHDW from Adam Tech

Figure 2.8: Front panel elements

Source (a): https://www.digikey.com/product-detail/en/keystone-electronics/7687/36-7687-ND/316787

Source (b): https://www.tme.eu/pl/Document/021bdd302fcfa7798d688ae3e277131c/RF2-49B-T-00-50-G-HDW.pdf

Usually, the SMA connector shield is connected directly to the system's ground. In such a case, when using multiple interconnected devices, cable shields can form closed loops through the power supply ground. Any strong magnetic fields (usually 50/60 Hz hum) can induce a noise voltage into the loop formed by the signal conductors and the power supplies[12][13]. To break these low-frequency noise loops, SMA connector grounds can be isolated by removing the $0\ \Omega$ resistors connecting them to the system ground (marked on the PCB with a letter 'G'). In this case, a $100\ k\Omega$ resistor in parallel with a $10\ nF$ capacitor creates the return path to the system ground for the high-frequency signal. The $100\ k\Omega$, so-called bleeding resistor removes ESD charges that could damage fragile RF circuits. In addition, the connectors must be isolated from the grounded front panel - for this reason, the device is fitted with *Keystone 7687* insulating washers.

When arranging the front panel elements, it was important to account for the size of SMA washers. The distance between the connectors must be greater than 11.1 mm (diameter of a single washer).

[8] One of standard Eurorack sizes - front panel dimensions are 20x128.4 mm

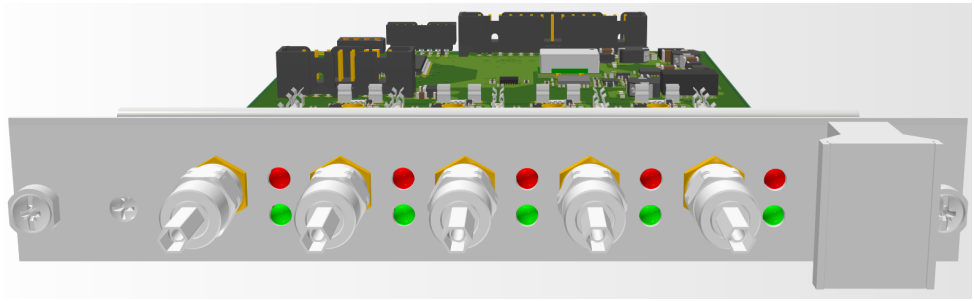


Figure 2.9: Front panel assembly render

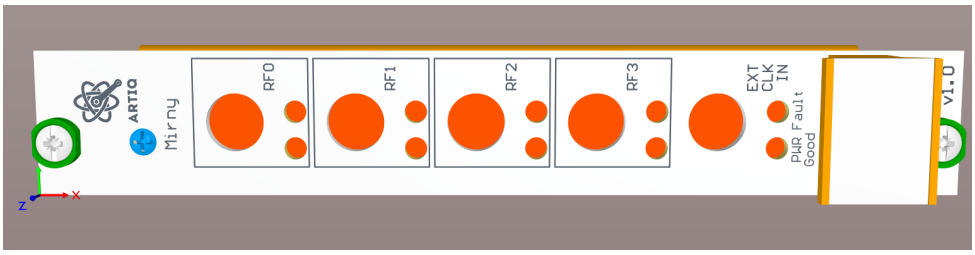


Figure 2.10: Front panel design

Additionally, if the connectors are placed too close then even with a separation of individual washers the LED indicators can be obstructed.

The front panel holes and silkscreen prints were laid out in the Altium Designer together with 3D models of cable assemblies, to confirm that access to the elements would not be obstructed by other front panel components (fig. 2.10). To take advantage of all the space available on the faceplate, SMA sockets and LEDs were equally spaced 8.38 mm apart.

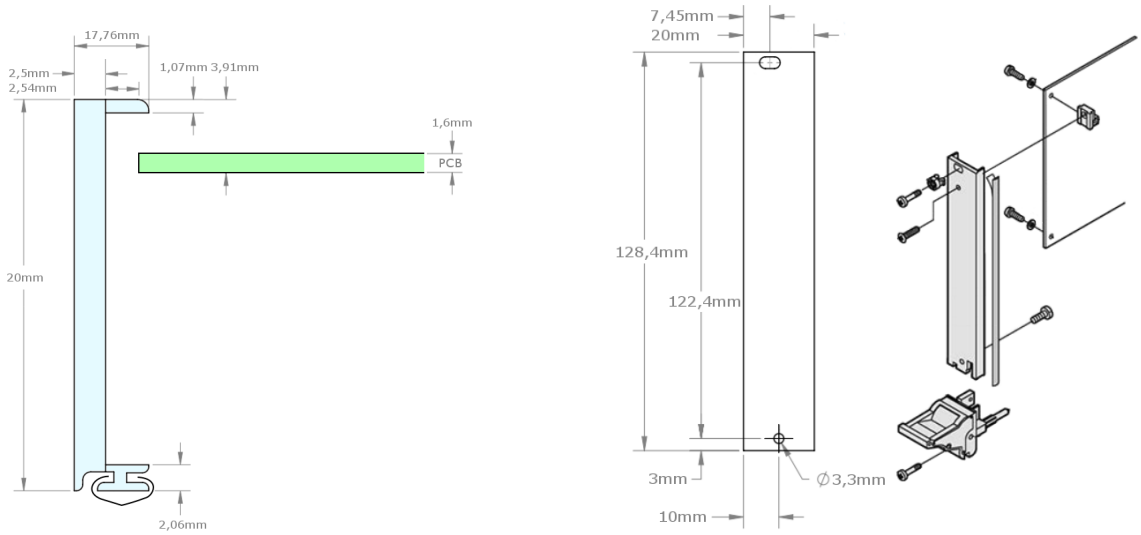


Figure 2.11: 3U4HP Front panel dimensions

Source (a): based on https://www.mouser.com/ds/2/424/-1109439.pdf

Source (b): based on https://docs-emea.rs-online.com/webdocs/14aa/0900766b814aabad.pdf

Phase Locked Loop

The project is based on four PLL-based microwave synthesizer chips, which can be used for the generation of independent output frequencies. In the ADF5356, the frequency reference signal is first passed through the adjustable input dividers and doubler:

$$f_{PFD} = REF_{IN} \cdot \frac{1+D}{R \cdot (1+T)}$$

Where:

REF_{IN} is the reference frequency,

D is the reference doubler bit,

R is the reference division factor,

T is the divide by 2 bit.

And then compared with divided VCO output in the phase detector:

$$RF_{OUT} = N \cdot f_{PFD}$$

$$RF_{OUT} = (INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1}) \cdot f_{PFD}$$

Where:

RF_{OUT} is the VCO frequency,

N is the frequency divider coefficient,

INT is the integer division factor,

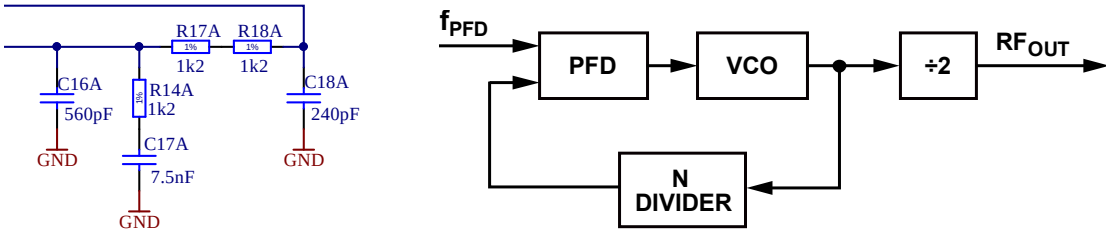
$FRAC1$ is the fractionality,

$FRAC2$ is the auxiliary fractionality,

$MOD1$ is the fixed 24-bit modulus,

$MOD2$ is the auxiliary modulus.

A phase difference between the output and the reference creates an error signal, which is then passed through the low pass filter and used to control the voltage controlled oscillator - locking the output frequency.



(a) PLL filter

(b) PLL block diagram

Figure 2.12: Phase locked loop in ADF5356 synthesizer

Phase noise is an important parameter when designing a PLL loop, as it has a significant impact on the noise of the entire system. The noise coming from the generator and the oscillator is passed through the dividers to the phase detector, from where it's passed through the low-pass filter of the feedback loop. As a result, those noise sources will be limited by the bandwidth of the filter and will appear on the tuning voltage at the generator. It is possible to limit the noise band by reducing the bandwidth of the loop filter. The disadvantage of this solution is an increase in the time needed to reach a stable state and the generation of the set frequency. This, however, is not the desired functionality in this project. The frequency division factor N also has a significant influence on the noise level. The synthesizer works on the principle of multiplication of the reference frequency, and thus reference noise is also multiplied (by $20 \cdot log\ N$). In order to minimize this noise, the multiplication factor N should be kept as low as possible. This can be achieved by selecting a higher reference frequency and a higher frequency[14] of the phase detector. The maximum operating frequency of the phase detector in the *ADF5356* synthesizer is 125 MHz. To reduce noise and simplify calculations of the divider value required for the generation of a set output frequency, a 100 MHz reference was selected.

The layout of components and their values were obtained using ADIsimPLL - a dedicated program supplied by Analog Devices (Fig. 2.12a). The design focused on the minimization of the phase noise and reusing elements already present in the system (eg R14, R17, R18). A reference frequency of 100 MHz, a filter bandwidth of 50 kHz and a phase margin of $45\,\mathrm{deg}$ were used in the calculation. The output frequency resolution achieved for each tuning range is presented in table 2.3.

Table 2.3: Frequency resolution for ADF5356

Start frequency	Stop frequency	Resolution
54,0 MHz	106,25 MHz	93,132 μHz
106,25 MHz	212,5 MHz	186,26 μHz
212,5 MHz	425 MHz	372,53 μHz
425 MHz	850 MHz	745,06 μHz
850 MHz	1,70 GHz	1,4901 mHz
1,7 GHz	3,4 GHz	2,9802 mHz
3,4 GHz	4,4 GHz	5,9605 mHz

Based on ADIsimPLL.

Internal frequency reference

The design requires a reference with high stability and low phase noise which would not degrade the PLL performance. The main source is an internal oscillator - 'CCHD-950-25-100.000' - with a frequency of 100MHz and precision of 2.5 ppm[9]. Two additional reference inputs are given as an SMA connector placed on the front panel and an MMCX connector located directly on the PCB. Selection between both inputs and the internal oscillator is enabled by two cascaded 2:1 multiplexers - Si53312-B-GM (IC13) and Si53340-B-GM (IC17). Table 2.4 illustrates the control signal state necessary for the selection of each input source.

The Si53312 multiplexer has a built-in frequency divider with possible values of 1/2/4 selected with a tri-state control signal. Thus, the frequency range of additional reference inputs (limited by the capabilities of IC13) is:

$$f_{inIC9} = 10\ MHz ... 600\ MHz$$
$$k = 1, 2, 4$$
$$f_{inIC9} = f_{weIC13}/k$$
$$f_{inIC13} = 10 ... 725\ MHz$$

where:

f_{inIC9} is the input frequency range of synthesizer chips,

f_{inIC13} is the input frequency range of *Si53312*,

k are the possible frequency divider values of *Si53312*.

Table 2.4: Reference source multiplexer - truth table

IN_SEL0	IN_SEL1	Source
0	0	internal oscillator
0	1	MMCX connector (J7)
1	0	SMA connector (J2)
1	1	SMA connector (J2)

[9] 'parts per million' - the precision of 1 ppm is equal to 0.0001%

Communication Interface

The main control unit of the module, responsible for virtually all other components, is the Xilinx XR2C128-6TQG144C CPLD[10]. The only exception is the power block and temperature sensor, managed via I2C directly by the EEM Carrier (e.g. Kasli[15]). Communication with the carrier is performed over the EEM connector - through the aforementioned I2C bus used for identification and fault detection and through 8 LVDS[11] lines. The first four lines are dedicated to the SPI bus, and the other four are dedicated for control of the output switches. Since the synthesizers use an interface very similar to the SPI, this greatly simplifies the operations performed by the CPLD.

Table 2.5: EEM connector pin assignment

Function	Comment	Pin number	Pin designation (SPI)
GND		1, 4, 7, 10, 13, 16, 19, 22, 25	
+12 V	max 2 A	28, 29	
+3,3 V	max 20 mA	30	
I2C	3,3 V LVCMOS	26 (SDA), 27 (SCL)	
LVDS 1	bi-directional LVDS	2 (P), 3(N)	SCLK, clock-capable
LVDS 2	bi-directional LVDS	5 (P), 6(N)	MOSI
LVDS 3	bi-directional LVDS	8 (P), 9(N)	MISO
LVDS 4	bi-directional LVDS	11 (P), 12(N)	CS0
LVDS 5	bi-directional LVDS	14 (P), 15(N)	CS1
LVDS 6	bi-directional LVDS	17 (P), 18(N)	
LVDS 7	bi-directional LVDS	20 (P), 21(N)	
LVDS 8	bi-directional LVDS	23 (P), 24(N)	

To provide logic compatibility between single-ended 3.3 V CMOS signals from the CPLD and LVDS signals from the EEM connector, two four-channel bi-directional buffers (IC1, IC6) were used. Data direction for each of the 8 control lines is determined by designated control signals from the CPLD.

Both the LVDS-CMOS buffers and the CPLD (IC10) have already been used in *Urukul 9910/9912 module*, and due to the similarity between the EEM cards, it was decided to reuse them. Though alternative solutions are available, the CPLD is a simple one which additionally provides the possibility of introducing minor post-production corrections and provides ease of future expansion or modification of the project's functionality.

[10] Complex Programmable Logic Device

[11] Low Voltage Differential Signal

Power supply

Not all voltage levels required for operation are supplied via the EEM connector (J1). Upon power-up, only the EEPROM with EUI-48 node identity (IC8) and thermal watch-dog (IC12) are directly supplied with low current 3,3 V rail. This ensures protection from thermal faults and identification of connected EEM card. All other necessary voltages: 3.3 V, 5.0 V, 5.5 V, 7.0 V, 7.5 V, 12 V, are created from 12 V supply rail provided by the EEM connector. Despite 3.3 V voltage being present at the EEM connector, its current capability would not be enough for the estimated consumption (as shown in table 2.5 and 2.6), thus a separate 3.3 V supply voltage is created from the 12 V rail.

Table 2.6: Maximum current drawn by individual components

Voltage level	3.3 V	3.3 V (A^1)	5 V (A^1)	5.5 V	7 V (A^1)	7.5 V	12 V
LVDS interface	378 mA	-	-	-	-	-	-
CPLD	100 mA	-	-	-	-	-	-
ADF5356	-	4·176.4 mA	4·78 mA	-	-	-	-
Si53340	-	140 mA	-	-	-	-	-
Si53312	-	240 mA	-	-	-	-	-
TCXO	-	6 mA	-	-	-	-	-
HMC542BLP4E	-	-	4·2.9 mA	-	-	-	-
HMC349LP4C	-	-	4·3.5 mA	-	-	-	-
ERA-4XSM+	-	-	-	-	4·85 mA	-	-
Optional AFE	400 mA	-	-	160 mA	-	400 mA	600 mA
Total	478 mA	1091.6 mA	337.6 mA	-	340 mA	-	-
Total with AFE	878 mA	1091.6 mA	337.6 mA	160 mA	340 mA	400 mA	600 mA

[1] Indicates a filtered rail for noise sensitive devices.

The power supply is built around three step-down converters which reduce the 12 V input supply to values close to target voltages: 3.6 V, 5.5 V and 7.5 V. Voltages are then passed through a set of low-dropout regulators, which create the required supply rails. Such design offers benefits of both switching converters and linear regulators: minimized power dissipation and low noise. The main switching converter is a dual buck LTM4622AEV (IC15), which creates 3.6 V and 7.5 V rails. Both outputs are enabled by thermal watchdog LM75 (IC12), ensuring proper operation and fault protection. The fault detection signal and its negation are additionally routed to a red and green LED on the front panel to indicate the power supply state directly to the user. Outputs then pass through TPS74901RGWT and LT1763CS8 LDO regulators, which create 3.3 V and 7.0 V supply rails. Remaining supply rails: 5.0 V and 5.5 V are created by second buck converter - TPS62175DQC (IC22) - followed by the LT1763CS8 LDO (IC20).

Frequency synthesizer chips, internal oscillator, and frequency reference multiplexers are powered with the 3.3 V supply, which is also required by the CPLD and LVDS buffers. To minimize noise coupled through the voltage rail, two 3.3 V LDO regulators were used to separate supply for sensitive components. Other AFE components do not share their power supply with the digital section, so no additional regulators were required.

The main 12 V supply provided via the EEM connector is limited to 2 A - higher current consumption would require the use of two or more EEM connectors. Since no additional control signals are required, and the synthesizer occupies a single rack slot (front panel width of 4HP), using additional EEM connectors would be wasteful. Maximum current consumption was estimated based on the power load of individual components summarized in table 2.6. The values were then used to calculate power losses of main power supply components (shown in table 2.7 and 2.8) - results have later also been used for the simulation of current density and voltage drop on PCB traces and for the thermal simulation.

Table 2.7: LDO regulator power load

Voltage rail	3.3 V	3.3 V (A)	5 V (A)	7 V (A)
Load power	1577 mW	3602 mW	1688 mW	2380 mW
Load power with AFE	2897 mW	3602 mW	1688 mW	2380 mW
Power loss	143.4 mW	327.5 mW	168.8 mW	170.0 mW
Power loss with AFE	263.4 mW	327.5 mW	168.8 mW	170.0 mW
Total consumption	1721 mW	3930 mW	1857 mW	2550 mW
Total consumption with AFE	3161 mW	3930 mW	1857 mW	2550 mW

$P_{load} = V_{out} \cdot I_{out}, \qquad P_{loss} = (V_{in} - V_{out}) \cdot I_{out}, \qquad P_{total} = P_{load} + P_{loss}.$

Table 2.8: Switching converter power load

Voltage rail	3.6 V	5.5 V	7.5 V
Load power	5651 mW	1857 mW	2550 mW
Load power with AFE	7091 mW	2737 mW	5550 mW
Power loss	627.8 mW	97.73 mW	283.3 mW
Power loss with AFE	787.8 mW	144.0 mW	616.7 mW
Total consumption	6278 mW	1955 mW	2833 mW
Total consumption with AFE	7878 mW	2881 mW	6167 mW

$P_{load} = V_{out} \cdot I_{out}, \qquad P_{loss} = (\frac{1}{\eta} - 1) \cdot P_{load}, \qquad P_{total} = P_{load} + P_{loss}.$

Hence the total power consumption of the synthesizer module is: 18.27 W (24.13 W with AFE), which equals 1.522 A (2.01 A with AFE), and one EEM connector is sufficient for the synthesizer module.

Based on results listed above, output current values of linear voltage regulators and switching converters were checked against their absolute maximum values (as listed in documentation provided by the manufacturers). Excessive current could activate internal overcurrent protection, shorten the life of the components or lead to an unpredictable behavior.

Table 2.9: Maximum voltage regulator current vs limiting value

Component	Voltage rail	Maximum current	limiting value
IC7 TPS74901RGWT (LDO)	3.3 V	0.878 A	3 A
IC11 TPS74901RGWT (LDO)	3.3 V (A)	1.092 A	3 A
IC20 LT1763CS8 (LDO)	5 V (A)	0.338 A	0.5 A
IC21 LT1763CS8 (LDO)	7 V (A)	0.340 A	0.5 A
IC15 LTM4622AEV (Switching converter)	3.6 V	1.970 A	2 A
IC22 TPS62175DQC (Switching converter)	5.5 V	0.498 A	0.5 A
IC15 LTM4622AEV (Switching converter)	7.5 V	0.740 A	2 A

Calculations assume the optional AFE is installed.

For ease of measurement and verification of the power supply, test points and LED indicators have been placed at each voltage rail. Uneven brightness or flickering of one of the LEDs would suggest incorrect voltage on one of the supply rails - current limiting resistors were chosen for LED currents of approximately 1 mA. To minimize the number of BOM lines in the project, resistor values already used in other parts of the design were chosen.

2.4 PCB Design

Mirny has been designed on a 1.6 mm thick, 4 layer PCB, with dimensions as specified by the EEM standard[15]: 100 mm x 160 mm. Layer stack parameters - dielectric constant, pre-preg[12] and core thickness - were chosen so that traces with controlled impedance could be easily created: with a standard impedance of 50 Ω for single-ended signals and 100 Ω for differential signals. To create unbroken signal return paths (with most traces placed on the first and third layer), the second layer was used as a ground plane. The distribution of supply rails, due to the number of different voltages and their spread across the board, would be very troublesome on a single, dedicated power plane layer. Thus, the power supply traces and polygon pours were divided across all 3 signal layers.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,034mm	3,5	
3	L1	Copper	0,035mm		
4	Dielectric1	FR4	0,180mm	3,66	
5	P2	Copper	0,035mm		
6	Dielectric 2	FR4	0,710mm	4,2	
7	L3	Copper	0,035mm		
8	Dielectric 3	FR4	0,450mm	4,2	
9	L4	Copper	0,035mm		
10	Bottom Solder	Solder Resist	0,034mm	3,5	
11	Bottom Overlay				

Figure 2.13: PCB stackup

The *Sinara* project assumes future use of a backplane connection board inside the enclosure - EEM modules and EEM carrier would be connected via common backplane PCB instead of IDC cables. Once it's implemented, all new modules will be equipped with a cPCI S.0. connector dedicated for the BP. To provide backward compatibility with existing modules, a low-cost EEM to cPCI adapter board was designed[16]. Therefore, the EEM connector and mounting holes need to be placed in the correct orientation and position near the board edge to account for the adapter. Since the conversion board is designed for modules with either 1 or 2 connectors, the PCB area specified for the second EEM connector cannot be populated by tall components (marked with white rectangle on PCB silkscreen layer).

Components were positioned so that standard-sized EMI[13] gaskets could be placed around the most crucial PCB sections (fig. 2.14a). Due to the high density of modules inside the enclosure, the high-frequency circuits could be a potential source/receiver of interference for neighboring modules. Dedicated shielding gaskets placed over synthesizers and analog paths are an easy solution to this problem. For ease of assembly and disassembly, dedicated Harwin mounting clips were used (fig. 2.14b). By default, both shields and clips are not mounted.

[12] 'Pre-impregnated' composite intermediate layer used to separate additional copper layers from core laminate

[13] Electro-Magnetic Interference

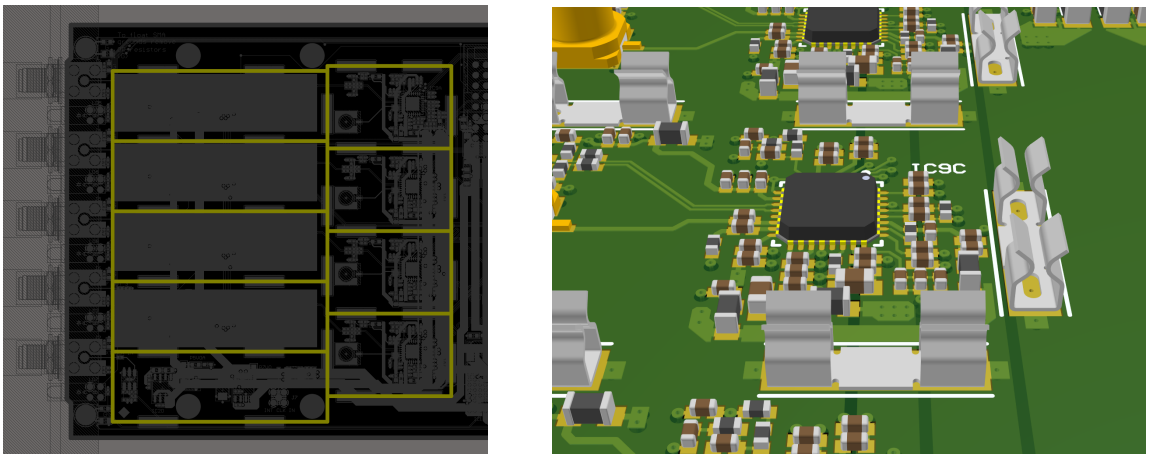


Figure 2.14: EMI shielding of the PCB RF sections

The EEM connector interface offers a high timing resolution. For the RF switches to still benefit from it, the propagation time of control signals on the module itself has to be equal across all channels. To even the propagation time, signal trace lengths: from the EEM connector LVDS[4..7] pins, via the LVDS buffer and the CPLD, to the RF switches, had to be matched (with a precision of 2.54 mm or 13.8 ps[17]). Additionally, the CPLD internal propagation time from EEM0[4..7] input to RFSW_CTRL[0..3] output has to be controlled as well. Since the optional AFE can be equipped with its own RF switches or other devices that would benefit from high timing resolution, signals between the CPLD and AFE connector have also been length-matched.

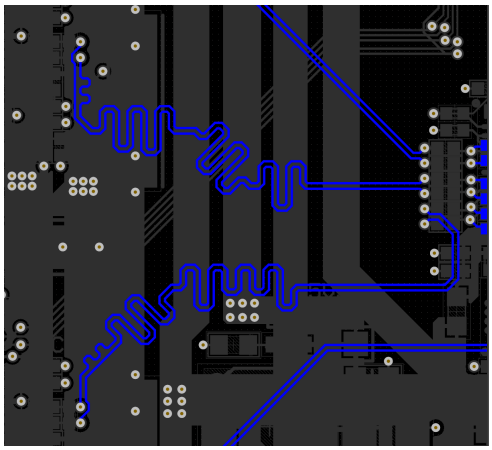


Figure 2.15: Length-matched traces

During PCB production, the weight difference of copper on a solid ground plane and signal layers could lead to bowing or twisting of the substrate or to uneven plating of vias and through-hole pads[18]. To reduce that risk, layer weight has been balanced - empty areas of signal layers were filled with copper.

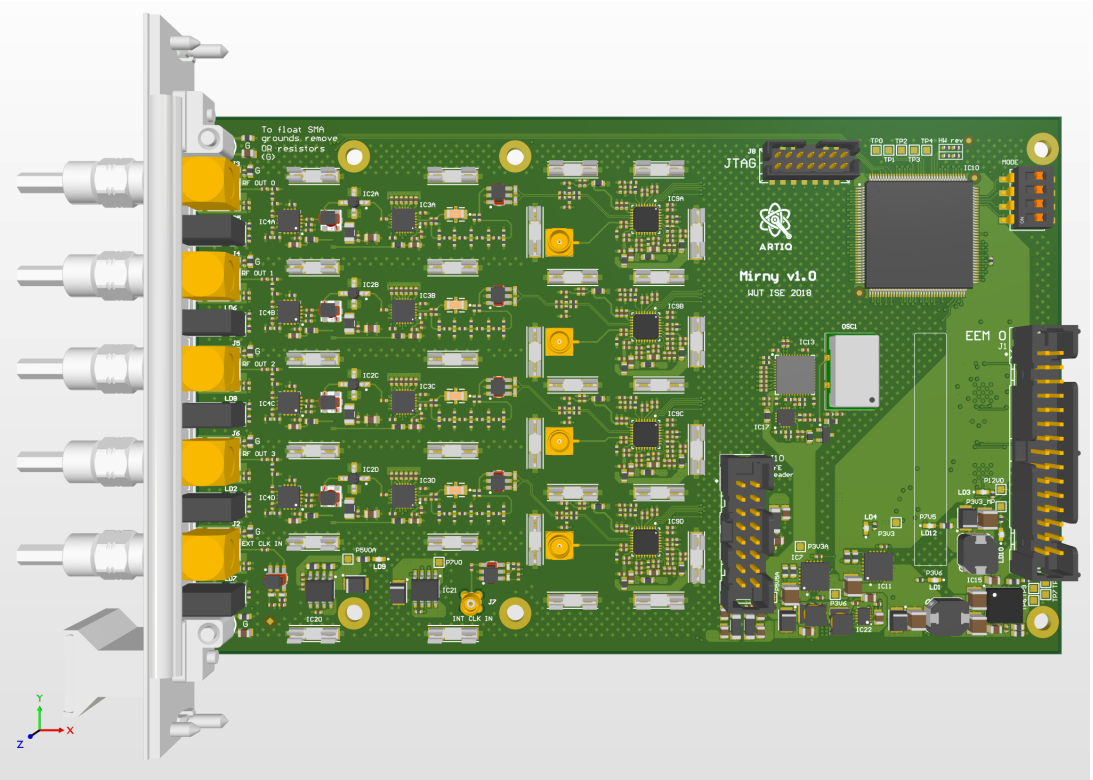


Figure 2.16: 3D model of designed PCB - top side

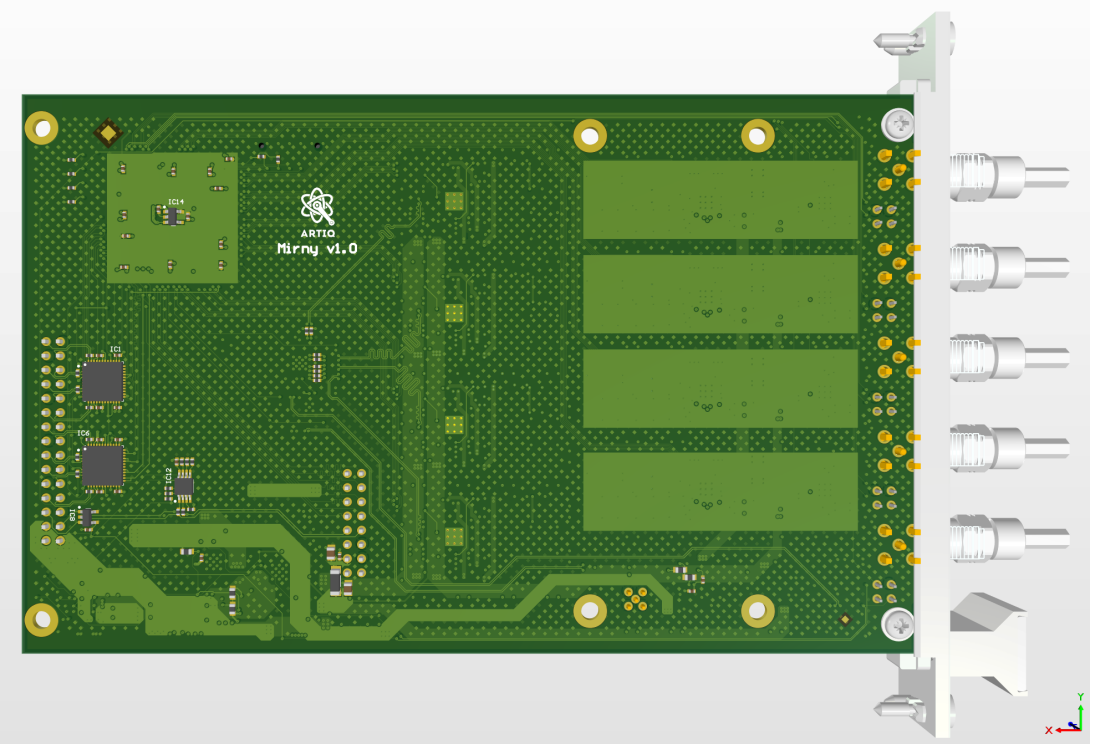


Figure 2.17: 3D model of designed PCB - bottom side

2.5 Project verification

The simulations concerned the most important parts of the design, in which errors were most likely to occur. Analysis regarded current density and voltage drops over the power supply connections and thermal performance of the module under full load. To carry out the PowerScope simulation with HyperLynx, the Altium PCB design file was exported to a compatible format. The full extent of simulation data is included in Appendix D.

Measurements for each supply rail aimed to determine the value and location of the highest voltage drops, which could cause improper operation. Excessive current density causes large drops on the resistance of the copper layers, which in turn leads to excessive heating of the substrate. Sufficiently large density may cause copper traces to burn, which would reduce the service life of the device. Thus the trace widths, copper pours and the number of vias[14] have been corrected so that for all voltage supply connections, current density does not exceed $50\ \frac{A}{mm^2}$. After the necessary design corrections, the highest current density of $46,97\ \frac{A}{mm^2}$ $(30,4\ \frac{mA}{mil^2})$ occurs on P5V5A rail. Supply voltage drops are within the range required for the correct operation of all components and do not exceed $38,4\ mV$.

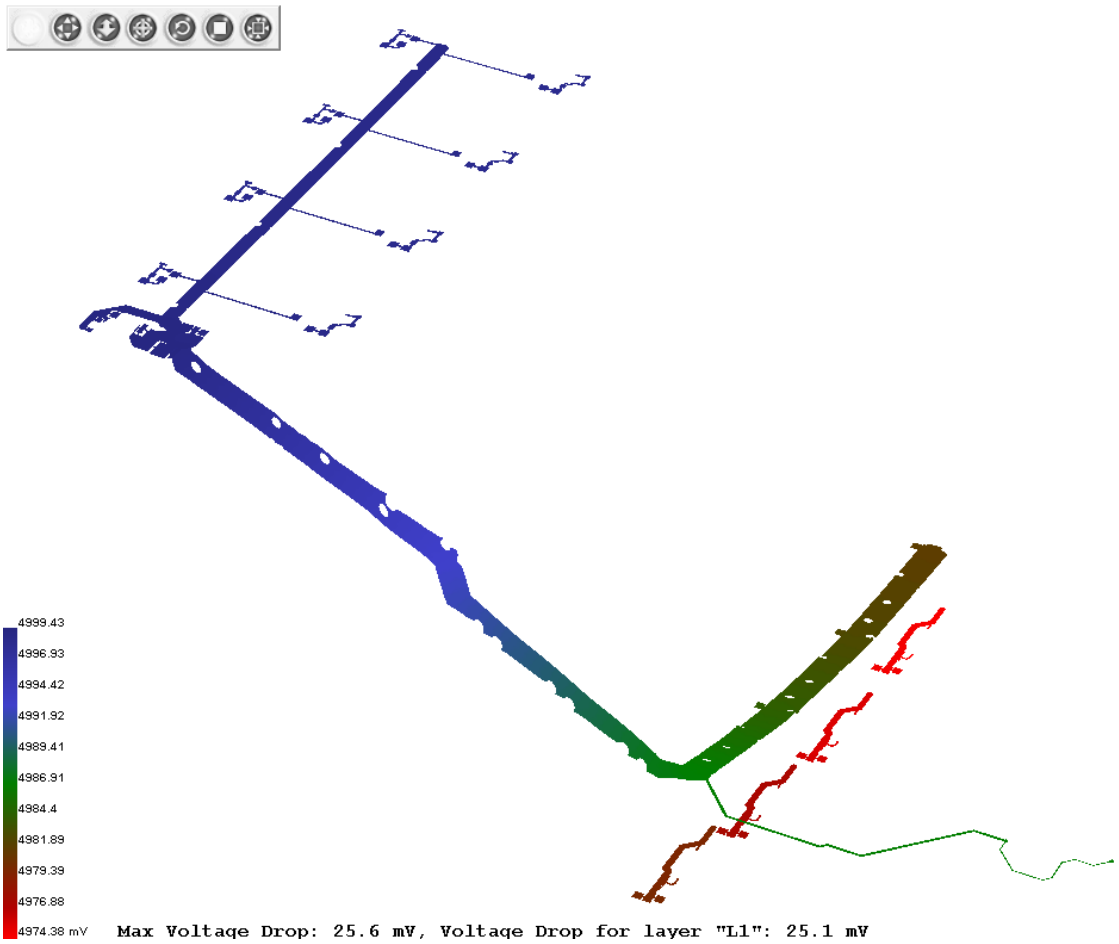
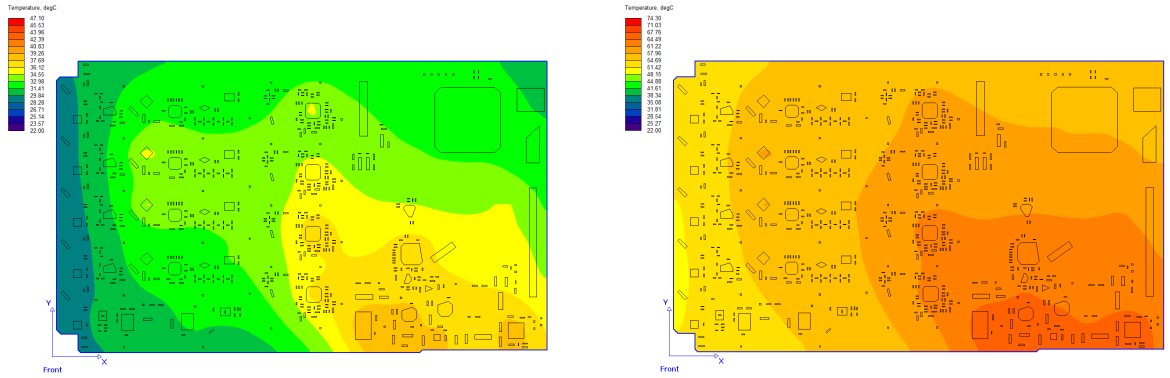


Figure 2.18: Voltage drop simulation of +5.0V supply rail

[14] 'Vertical Interconnect Access' - an electrical connection between PCB layers

The frequency synthesizer module is intended to be used either stand-alone in an enclosure or with other devices mounted in a standard 19" rack[15]. Thermal analysis allows estimating air circulation necessary for proper operation. The simulation assumed the worst possible environment conditions: a closed chassis with other devices. With an airflow of 130 $\frac{cm}{s}$ (fig. 2.19a) and ambient temperature of 22°C, the hottest element on the board is the IC27 multiplexer reaching 47,2°C. Thermal watchdog LM75 will turn the entire module off upon reaching 80°C, which would occur at airspeed of roughly 25 $\frac{cm}{s}$ (fig. 2.19b).



(a) airflow of 130 cm/s

(b) airflow of 25 cm/s

Figure 2.19: Thermal simulation in enclosed environment

3. Tests

During the prototype tests, the Mirny module was controlled with a modified EVAL-ADF4351 development board. The on-board ADF4351 chip was disconnected by removing series 0 Ω resistors on the SPI interface[19] so that the controller could be used to interface the module with a computer. Control software for EVAL-ADF4351 board does not support ADF5356 synthesizer, however, the development boards for the entire family of chips use the same controller circuitry. Since the original ADF4351 synthesizer chip was effectively replaced with ADF5356 synthesizer chips used on Mirny, software for EVAL-ADF5356 boards could be used to control the device. To convert TTL signals from the evaluation board controller to LVDS signals used by EEM modules, 3U_Tester_TTL logic level translator board was used[20]. The test set-up is illustrated in fig. 3.1.

The CPLD was configured to pass signals from EEM connector directly to ADF5356 chips, with a connection of each channel determined by the SW1 switch position. This allowed for setting individual or multiple chips at once. Full Verilog code used during testing is included in appendix E.

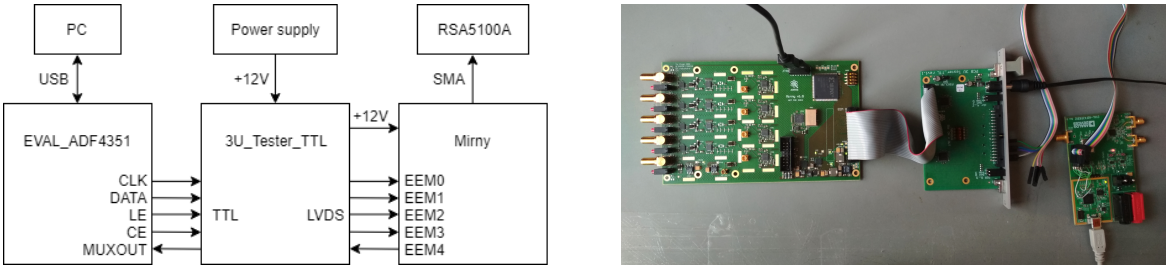


Figure 3.1: Test setup

After powering up and confirming the presence of all power rails, the synthesizer was connected to the RSA5100A spectrum analyzer. The SMA cable nuts were tightened with a fixed-torque wrench. Then, using the evaluation software and spectrum analyzer, each of the four channels was set to a few random frequencies and confirmed to lock at a correct value.

The CLK_DIV signal driving input reference divider in the Si53312 multiplexer (IC13) is driven by a tri-state CPLD output buffer. Depending on the value, the divider can be set to either[21]:

- divide by 1 (high-Z output),
- divide by 2 (logic 0 output),
- divide by 4 (logic 1 output).

For the best performance of the PLL, the input reference frequency was set to 100 MHz:

- multiplexer divider set to 1 (CLK_DIV set to high-Z),
- ADF5356 divider disabled,
- ADF5356 doubler disabled.

After power-up, the CLK_DIV net floats to $2,8\ V$ instead of $1,75\ V$, causing the multiplexer to divide reference by 4. Probing the CPLD side of the R89 resistor or connecting any additional capacitance to the net fixes the problem, and CLK_DIV is driven correctly until power-down. This is most likely caused by initial leakage in the CPLD output buffer, which overpowers internal bias resistors in Si53312 multiplexer. To prevent this from happening, the CPLD code should include a power-up routine of cycling through possible values of CLK_DIV net, which would force the signal to correctly bias the multiplexer. For the duration of the tests, CPLD code was modified to set division by 2 in the frequency reference multiplexer (logic 0 on CLK_DIV). To create the PFD frequency of 100 MHz required by the PLL design, the ADF5356 reference doubler was enabled.

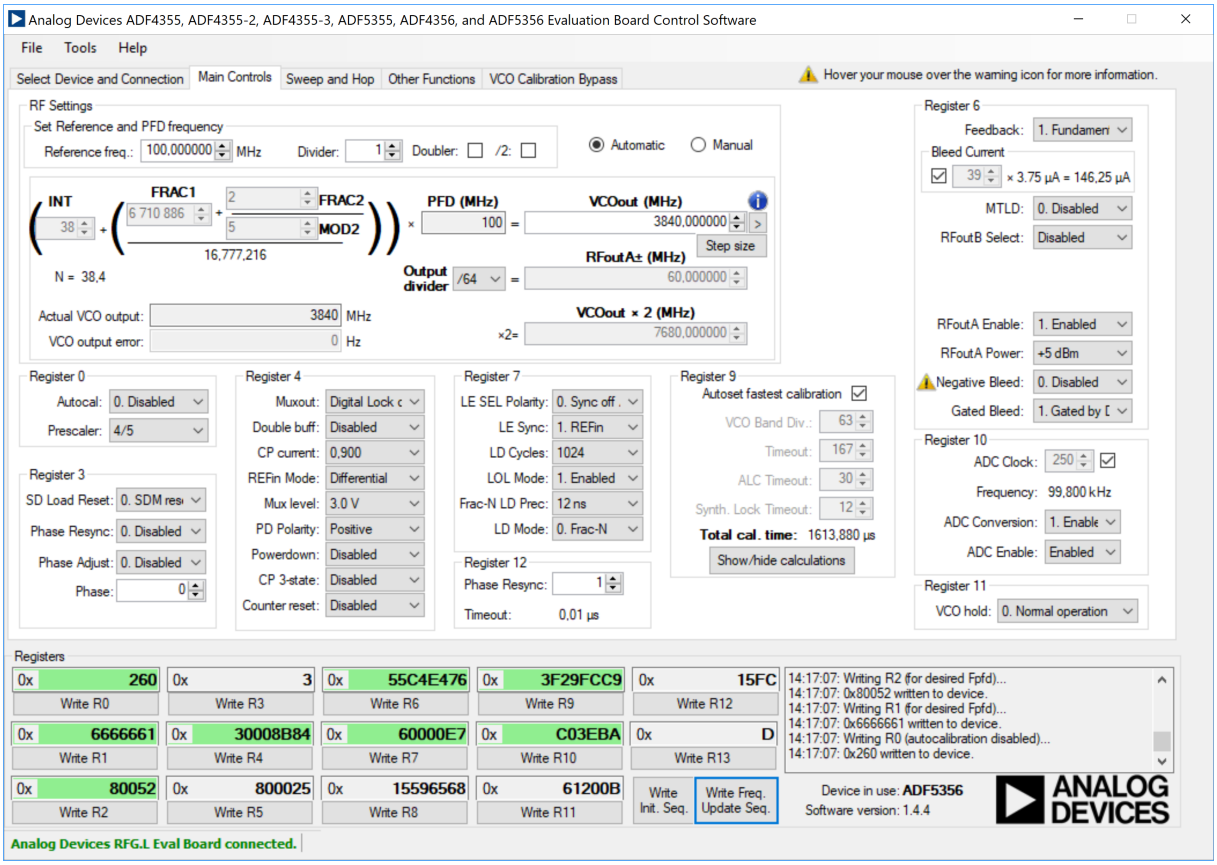
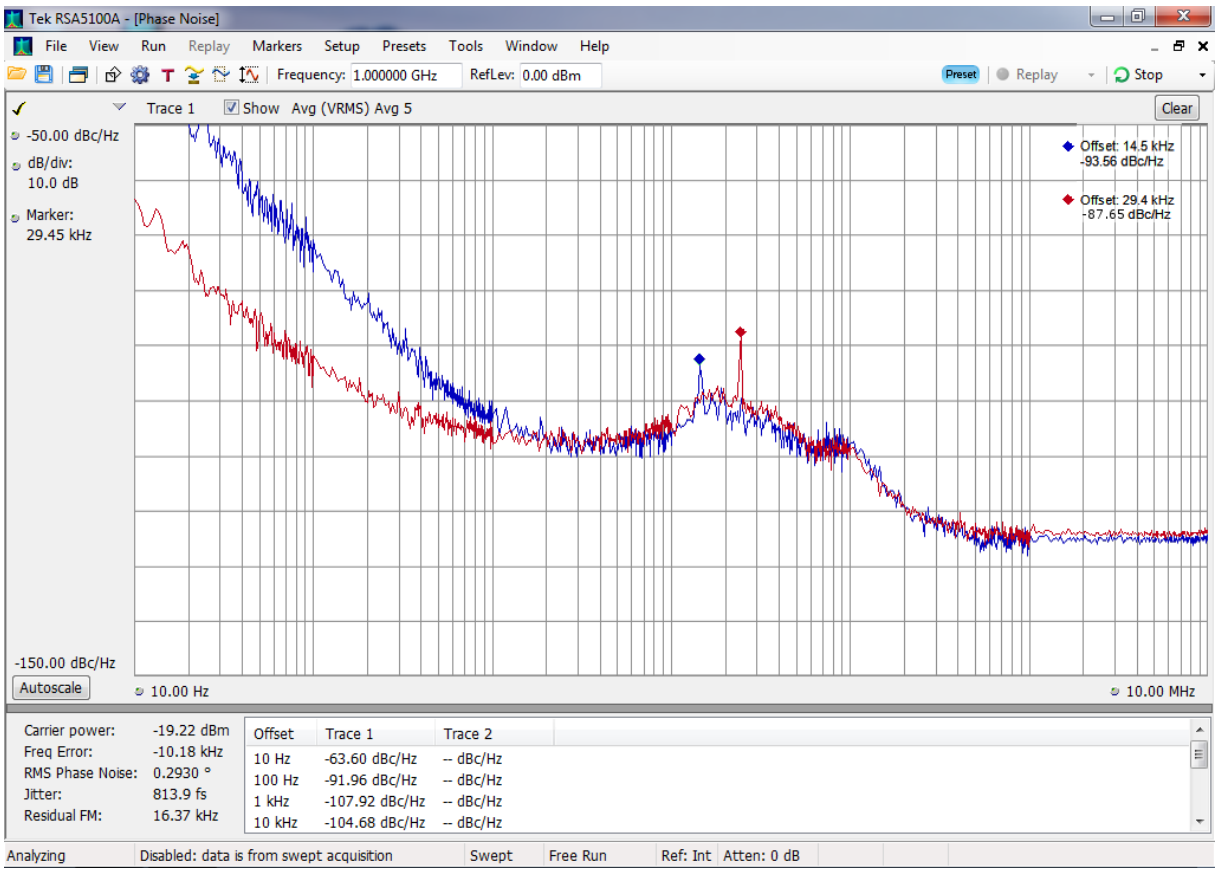


Figure 3.2: Evaluation board control software[22]

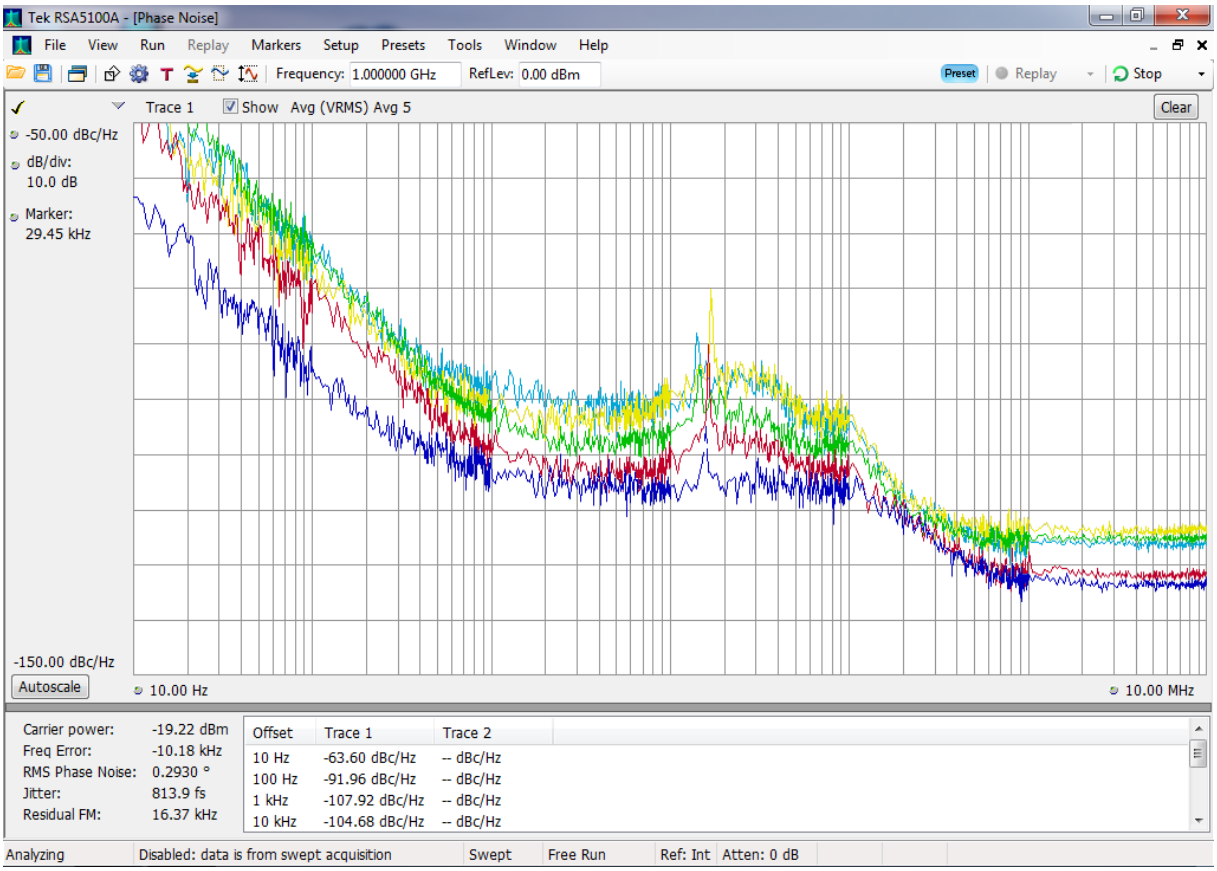
Output phase noise measurement was conducted at frequencies of 125 MHz, 500 MHz, 1 GHz, 2 GHz, and 3.5 GHz. Initial results showed a large noise response spike at 29.4 kHz. An oscilloscope was used to measure noise on supply rails, as switching converters used in the design could be a likely cause. This showed, that a ground loop consisting of the power supply, Mirny module, and the spectrum analyzer picked up and injected this noise frequency into the voltage supply. To break the loop path, a common mode choke was inserted between the power supply and the module. Additionally, to prevent switching regulators from oscillating, a 100 μF capacitor was connected to the output of the CM choke. This reduced the peak magnitude and lowered its frequency, slightly reduced overall noise floor and widened the slope of the carrier frequency (fig. 3.3).



Noise response legend: red - before installation of CM choke; blue - after installation of CM choke

Figure 3.3: Phase noise at 1 GHz output

The shape of the phase noise response coincides with the response characteristic of PLL synthesizers: with a pronounced step caused by the phase detector and charge pump, peaking at a bandwidth of the loop filter. The magnitude of in-band and wideband noise changes with output divider setting, with lower noise at higher divider value (lower output frequency), as stated in the ADF5356 datasheet. Overall performance, however, is worse than expected - due to the higher noise floor and visible 14.5 kHz spur.



Noise response legend: 125 MHz - blue; 500 MHz - red; 1 GHz - green; 2 GHz - yellow; 3.5 GHz - teal

Figure 3.4: Phase noise measurement

Table 3.1: Phase noise performance

Carrier offset	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
125 MHz output	-114 dBc/Hz	-116 dBc/Hz	-115 dBc/Hz	-132 dBc/Hz	-133 dBc/Hz
500 MHz output	-107 dBc/Hz	-129 dBc/Hz	-111 dBc/Hz	-130 dBc/Hz	-132 dBc/Hz
1 GHz output	-102 dBc/Hz	-106 dBc/Hz	-107 dBc/Hz	-125 dBc/Hz	-125 dBc/Hz
2 GHz output	-102 dBc/Hz	-98 dBc/Hz	-104 dBc/Hz	-123 dBc/Hz	-124 dBc/Hz
3,5 GHz output	-96 dBc/Hz	-101 dBc/Hz	-103 dBc/Hz	-127 dBc/Hz	-128 dBc/Hz

4. Summary

Tests of the Mirny synthesizer prototype confirm that it works as intended - fulfilling all of the design requirements - and is suitable for use in the experiments. Solutions used in the design offer high elasticity of desired performance and a path for future expansion, allowing for usage in fields other than initially intended, if frequency generation is required.

Control of synthesizer EEM now has to be integrated into the ARTIQ software, so that Mirny can be used with other devices in the Sinara ecosystem. The instrument should also be tested in a controlled environment, to determine and eliminate the source of 14.5 kHz spur visible in the phase noise and to possibly lower the phase noise floor.

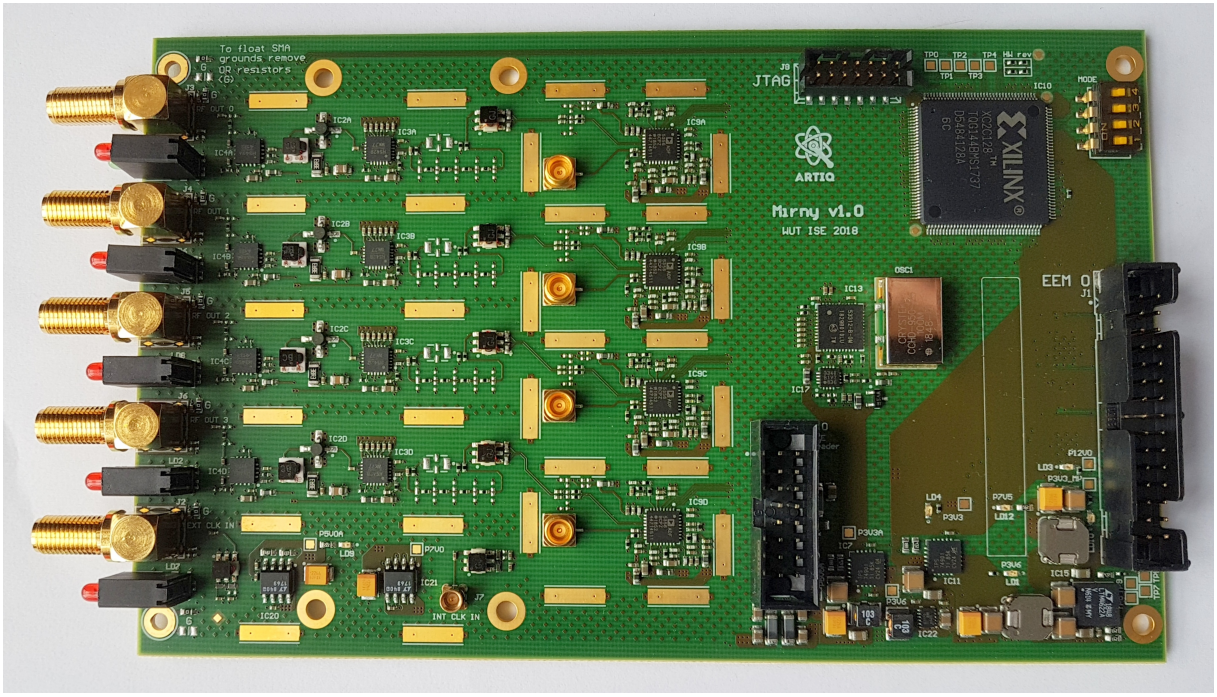


Figure 4.1: Assembled device

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List of symbols and abbreviations

AFE - Analog Front End.

AOM - Acousto-Optic modulator.

CM - Common Mode.

CPLD - Complex Programmable Logic Device.

EEM - Eurocard Extension Module.

EMI - Electro-Magnetic Interference.

EOM - Electro-Optic modulator.

I^2C - Inter-Integrated Circuit.

IDC - Insulation Displacement Connector.

JTAG - Joint Test Action Group.

LED - Light Emitting Diode.

LDO - Low Drop-Out.

LVCMOS - Low Voltage CMOS.

LVDS - Low Voltage Differential Signal.

PCB - Printed Circuit Board.

PFD - Phase/Frequency Detector.

PLL - Phase Locked Loop.

ppm - parts per milion.

SPDT - Single Pole Double Throw.

SPI - Simple Peripheral Interface.

VCO - Voltage Controlled Oscillator.

VIA - Vertical Interconnect Access

List of Figures

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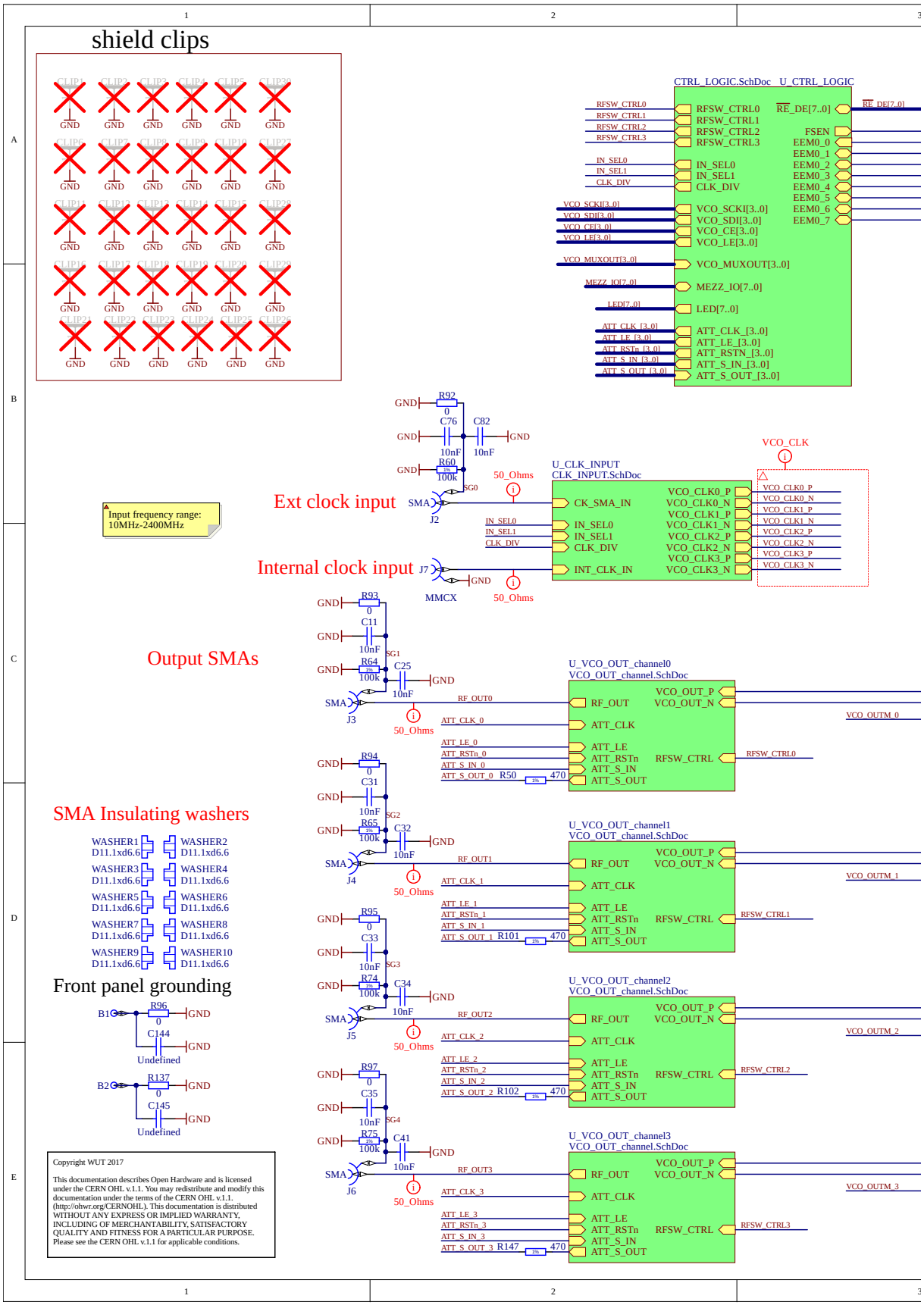
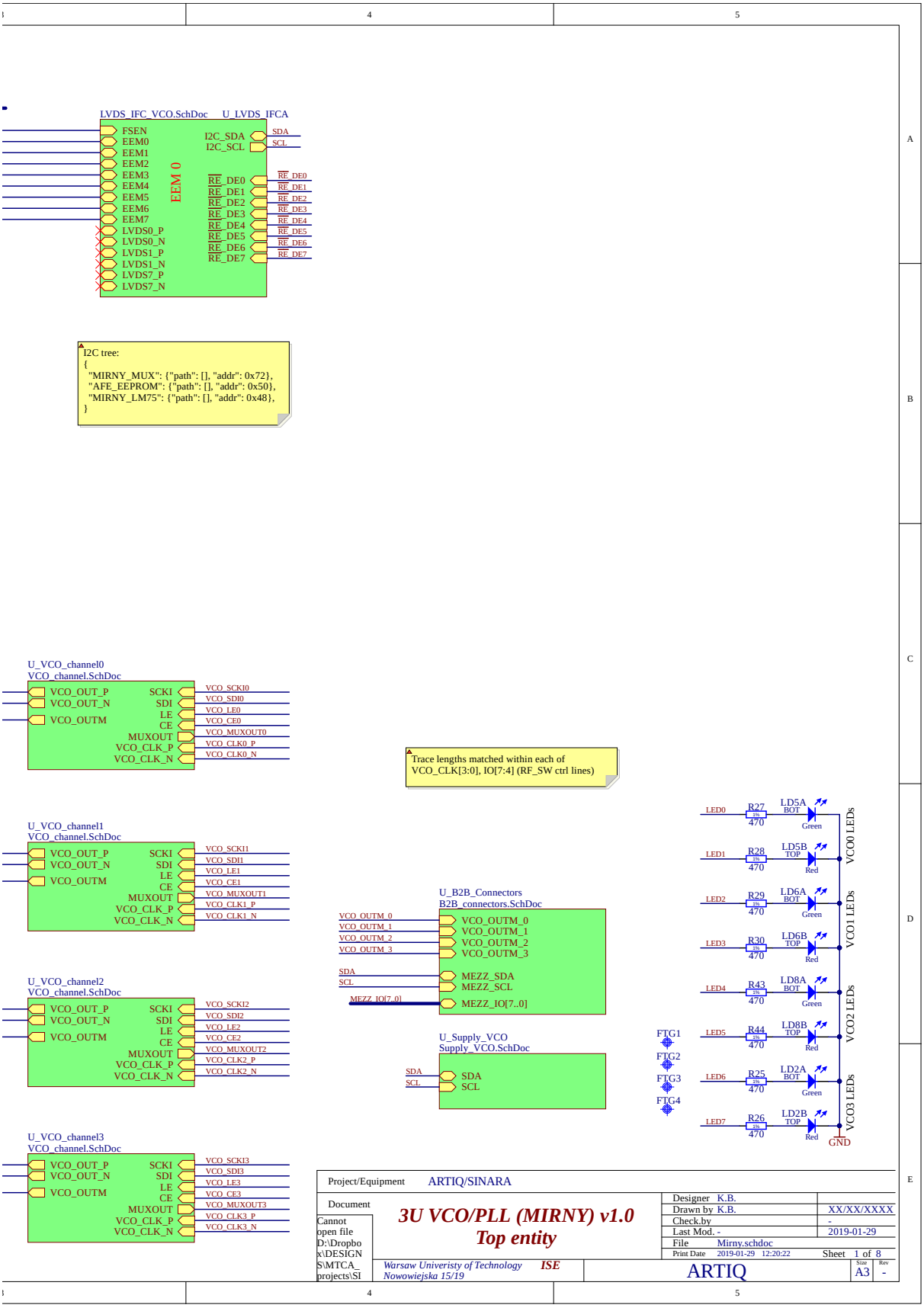
8.1 Appendix A - Schematics

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U_LVDS_IFCA
FSEN
EEM0
EEM1
EEM2
EEM3
EEM4
EEM5
EEM6
EEM7
LVDS0_P
LVDS0_N
LVDS1_P
LVDS1_N
LVDS7_P
LVDS7_N
EEM 0
I2C_SDA
I2C_SCL
SDA
SCL
RE_DE0
RE_DE1
RE_DE2
RE_DE3
RE_DE4
RE_DE5
RE_DE6
RE_DE7
I2C tree:
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"AFE_EEPROM": {"path": [], "addr": 0x50},
"MIRNY_LM75": {"path": [], "addr": 0x48},
}
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VCO_OUT_N
VCO_OUTM
SCKI
SDI
LE
CE
MUXOUT
VCO_CLK_P
VCO_CLK_N
VCO_SCKI0
VCO_SDI0
VCO_LE0
VCO_CE0
VCO_MUXOUT0
VCO_CLK0_P
VCO_CLK0_N
U_VCO_channel1
VCO_channel.SchDoc
VCO_SCKI1
VCO_SDI1
VCO_LE1
VCO_CE1
VCO_MUXOUT1
VCO_CLK1_P
VCO_CLK1_N
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VCO_channel.SchDoc
VCO_SCKI2
VCO_SDI2
VCO_LE2
VCO_CE2
VCO_MUXOUT2
VCO_CLK2_P
VCO_CLK2_N
U_VCO_channel3
VCO_channel.SchDoc
VCO_SCKI3
VCO_SDI3
VCO_LE3
VCO_CE3
VCO_MUXOUT3
VCO_CLK3_P
VCO_CLK3_N
Trace lengths matched within each of
VCO_CLK[3:0], IO[7:4] (RF_SW ctrl lines)
U_B2B_Connectors
B2B_connectors.SchDoc
VCO_OUTM_0
VCO_OUTM_1
VCO_OUTM_2
VCO_OUTM_3
SDA
SCL
MEZZ_IO[7..0]
MEZZ_SDA
MEZZ_SCL
U_Supply_VCO
Supply_VCO.SchDoc
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
R27
R28
R29
R30
R43
R44
R25
R26
470
LD5A
LD5B
LD6A
LD6B
LD8A
LD8B
LD2A
LD2B
BOT
TOP
Green
Red
VCO0 LEDs
VCO1 LEDs
VCO2 LEDs
VCO3 LEDs
FTG1
FTG2
FTG3
FTG4
GND
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ARTIQ/SINARA
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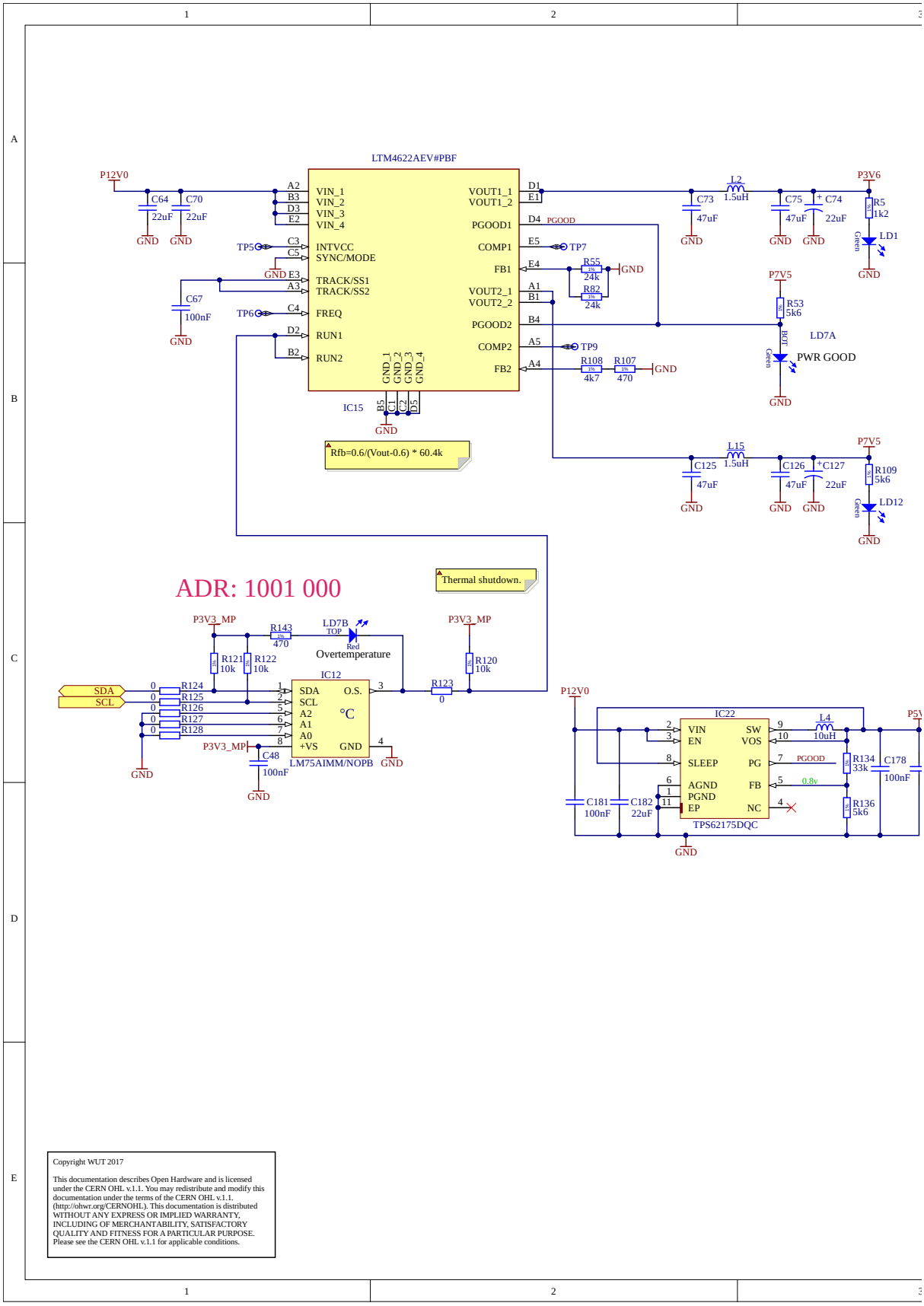
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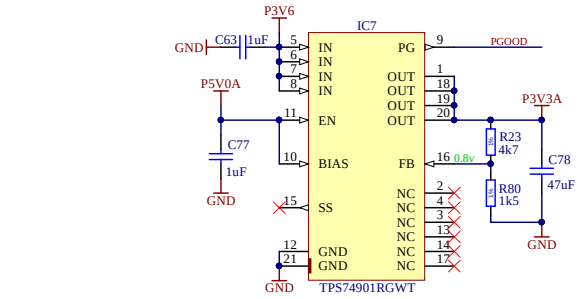
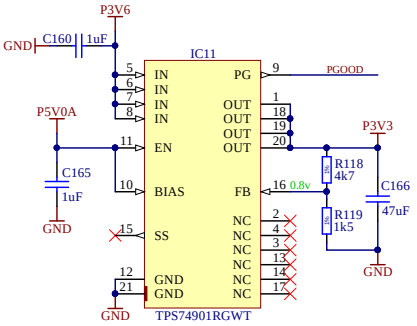
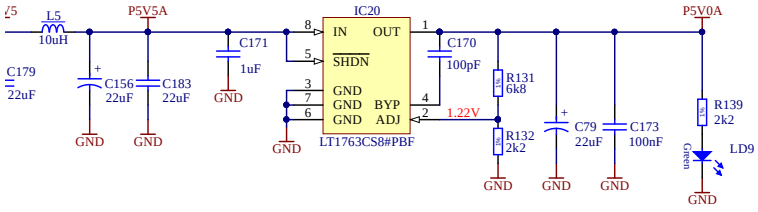
C64
22uF
C70
22uF
GND
VIN_1
VIN_2
VIN_3
VIN_4
INTVCC
SYNC/MODE
TRACK/SS1
TRACK/SS2
FREQ
RUN1
RUN2
VOUT1_1
VOUT1_2
PGOOD1
COMP1
FB1
VOUT2_1
VOUT2_2
PGOOD2
COMP2
FB2
TP5
TP6
TP7
TP9
C67
100nF
R55
24k
R82
24k
R108
4k7
R107
470
IC15
Rfb=0.6/(Vout-0.6) * 60.4k
L2
1.5uH
C73
47uF
C75
47uF
C74
22uF
P3V6
R5
1k2
LD1
P7V5
R53
5k6
LD7A
PWR GOOD
L15
1.5uH
C125
47uF
C126
47uF
C127
22uF
R109
5k6
LD12
ADR: 1001 000
Thermal shutdown.
P3V3_MP
R143
470
LD7B
Red
Overtemperature
R121
10k
R122
10k
R120
10k
R123
0
SDA
SCL
R124
R125
R126
R127
R128
IC12
O.S.
°C
+VS
C48
100nF
LM75AIMM/NOPB
IC22
VIN
EN
SLEEP
AGND
PGND
EP
SW
VOS
PG
FB
NC
L4
10uH
PGOOD
0.8v
R134
33k
C178
100nF
R136
5k6
C181
100nF
C182
22uF
TPS62175DQC
Copyright WUT 2017
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

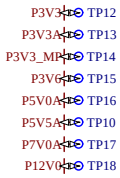


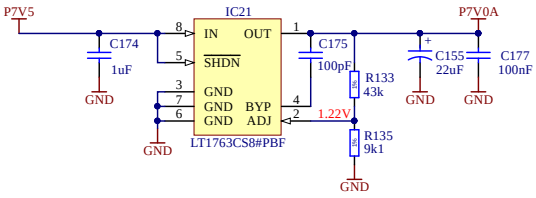


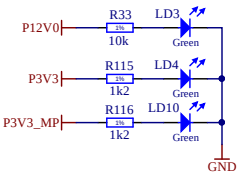
Power budget (max ratings):

P3V3:		
LVDS interface 2x	330	mA
LVDS load 2x24mA	48	mA
CPLD	100	mA
ADF5356	4*(176.4)=705,6	mA
Si53340-B-GM	140	mA
Si53312-B-GM	4*(35)+100=240	mA
TCXO	6	mA
TCA9548ARGER	10	mA
TOTAL P3V3	1579,6	mA
TOTAL POWER	5,213	W
P5V0:		
HMC542BLP4E	4*2,9=11.6	mA
HMC349LP4C	4*3,5=14	mA
ADF5356	4*(78)=312	mA
TOTAL 5V0	337,6	mA
TOTAL POWER	1,688	W
P7V0:		
ERA-4XSM+	4*85=340	mA
TOTAL 7V0	340	mA
TOTAL POWER	2,38	W
DC/DC converter losses		
TPS62175 eff .95	0,05*(0,338)*5,5=0,093	W
LTM4622:3.6V eff .9	0,1*1,557*3,6=0,569	W
LTM4622:7.5V eff .9	0,1*0,366*7.5=0,255	W
LDO losses		
3.6V->3.3V	0,474	W
5.5V->5V	0,169	W
7.5V->7V	0,17	W
(without AFE mezzanines)		
Total power from 12V	12,47	W
Total current from 12V	1,039	A
AFE mezzanines:		
P12V0:	4*150=600	mA
P7V5:	4*100=400	mA
P5V5:	4*40=160	mA
P3V3:	4*100=400	mA
Total power from 12V	23,99	W
Total current from 12V	1,999	A









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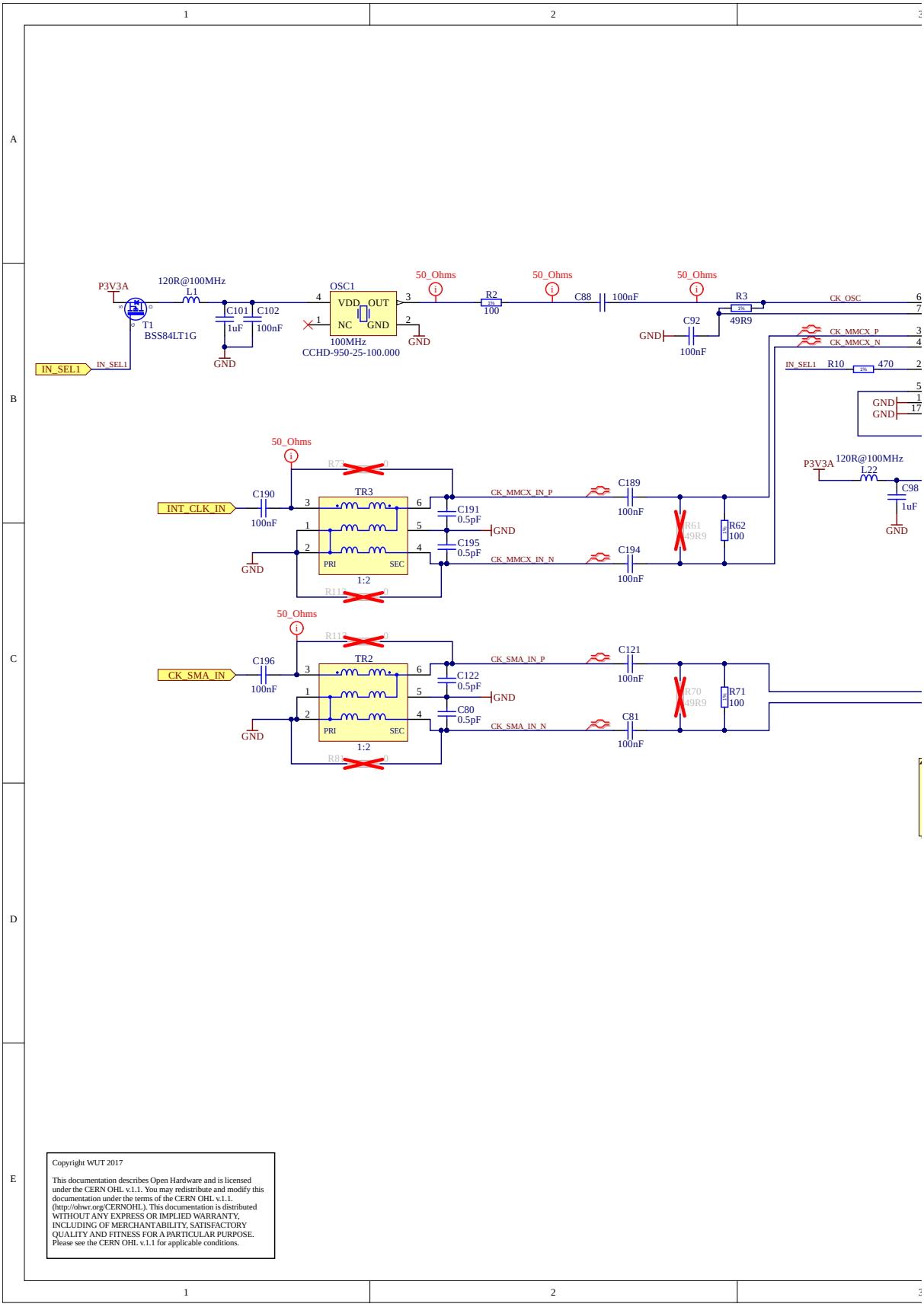

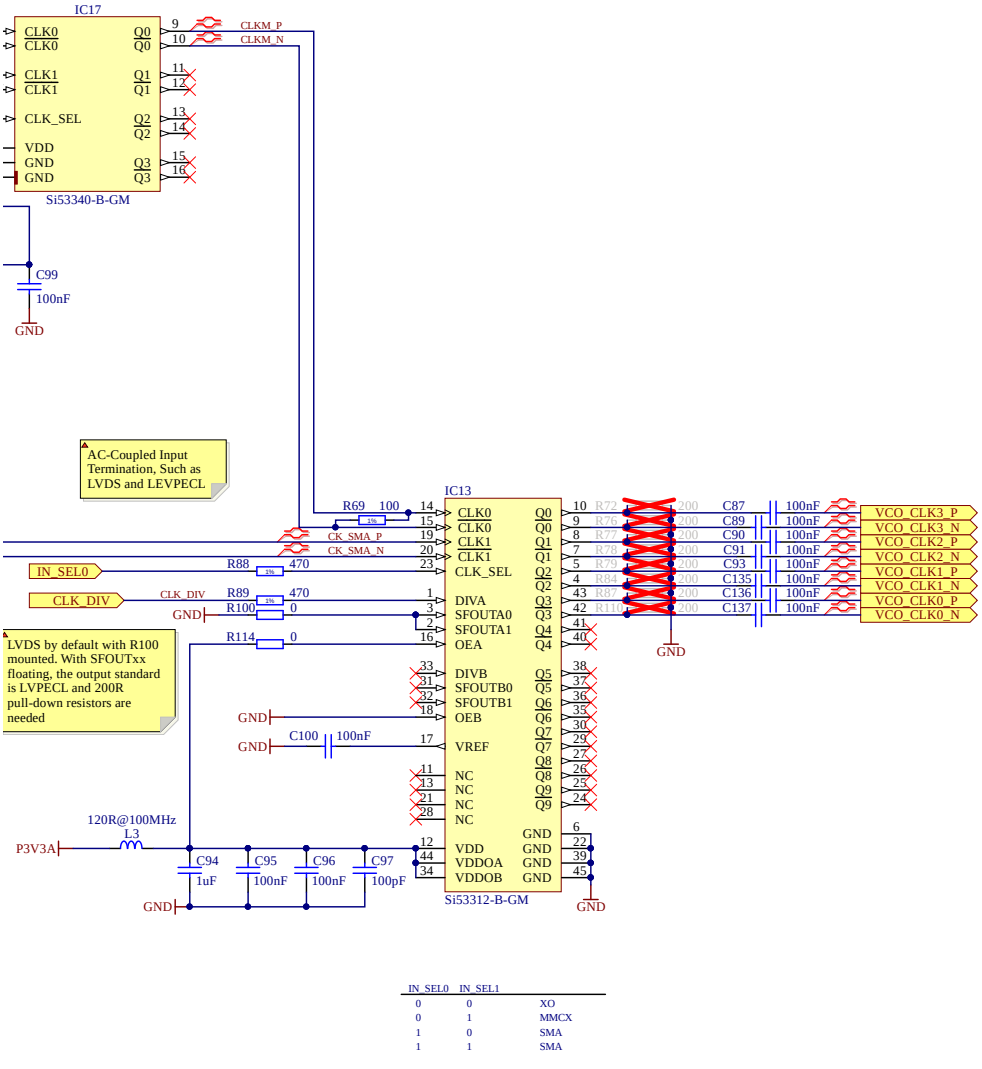

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0	1	MMCX
1	0	SMA
1	1	SMA

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$$RF_{OUT} = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \times (f_{PFD})/RF\ Divider$$

where:

RF_{OUT} is the RF frequency output.
INT is the integer division factor.
$FRAC1$ is the fractionality.
$FRAC2$ is the auxiliary fractionality.
$MOD2$ is the auxiliary modulus.
$MOD1$ is the fixed 24-bit modulus.
RF Divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T)))$$

where:

REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
R is the RF reference division factor.
T is the reference divide by 2 bit (0 or 1).

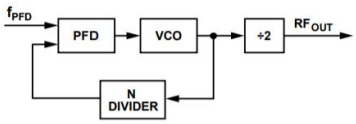
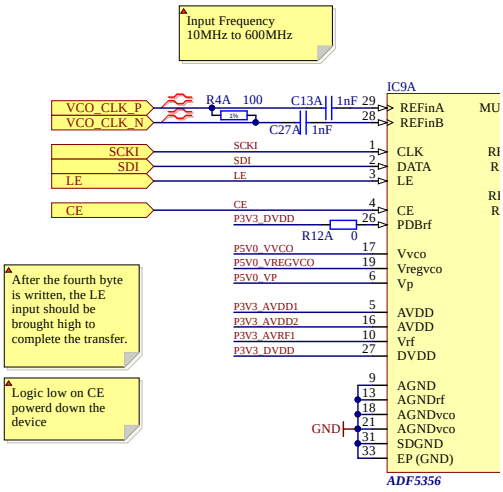
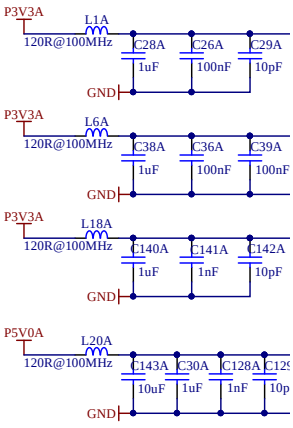
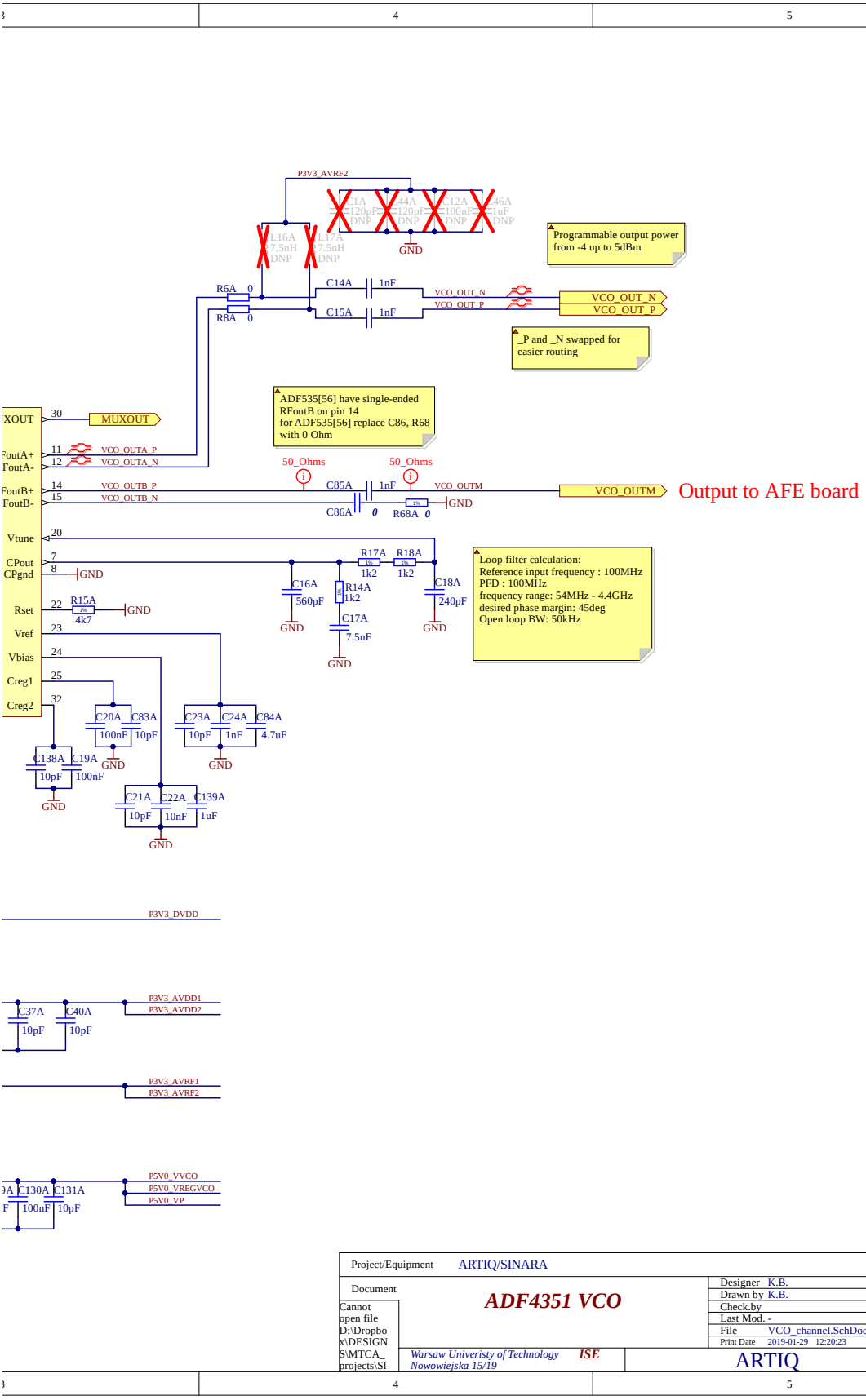


Figure 43. Loop Closed Before Output Divider

Start Freq	Stop Freq	VCO Divider	Channel Spacing
54.0MHz	106.25MHz	64	93.132uHz
106.25MHz	212.5MHz	32	186.26uHz
212.5MHz	425MHz	16	372.53uHz
425MHz	850MHz	8	745.06uHz
850MHz	1.70GHz	4	1.4901mHz
1.70GHz	3.40GHz	2	2.9802mHz
3.40GHz	4.40GHz	1	5.9605mHz



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C21A 120pF DNP
C44A 120pF DNP
C12A 100nF DNP
C46A 1uF DNP
GND
L16A 7.5nH DNP
L17A 7.5nH DNP
Programmable output power from -4 up to 5dBm
R6A 0
R8A 0
C14A 1nF
C15A 1nF
VCO_OUT_N
VCO_OUT_P
_P and _N swapped for easier routing
ADF535[56] have single-ended RFoutB on pin 14
for ADF535[56] replace C86, R68 with 0 Ohm
XOUT
30
MUXOUT
FoutA+
FoutA-
11
12
VCO_OUTA_P
VCO_OUTA_N
50_Ohms
50_Ohms
FoutB+
FoutB-
14
15
VCO_OUTB_P
VCO_OUTB_N
C85A 1nF
C86A 0
R68A 0
VCO_OUTM
Output to AFE board
Vtune
20
CPout
CPgnd
7
8
R17A 1k2
R18A 1k2
C16A 560pF
R14A 1k2
C17A 7.5nF
C18A 240pF
Loop filter calculation:
Reference input frequency : 100MHz
PFD : 100MHz
frequency range: 54MHz - 4.4GHz
desired phase margin: 45deg
Open loop BW: 50kHz
Rset
22
R15A 4k7
Vref
23
Vbias
24
Creg1
25
Creg2
32
C20A 100nF
C83A 10pF
C23A 10pF
C24A 1nF
C84A 4.7uF
C138A 10pF
C19A 100nF
C21A 10pF
C22A 10nF
C139A 1uF
P3V3_DVDD
C37A 10pF
C40A 10pF
P3V3_AVDD1
P3V3_AVDD2
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Warsaw Univeristy of Technology ISE
Nowowiejska 15/19
ARTIQ
Size A3
Rev -

$$RF_{OUT} = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \times (f_{PFD})/RF\ Divider$$

where:

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FRAC1 is the fractionality.
FRAC2 is the auxiliary fractionality.
MOD2 is the auxiliary modulus.
MOD1 is the fixed 24-bit modulus.
RF Divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T)))$$

where:

REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
R is the RF reference division factor.
T is the reference divide by 2 bit (0 or 1).

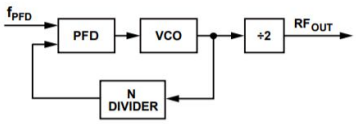
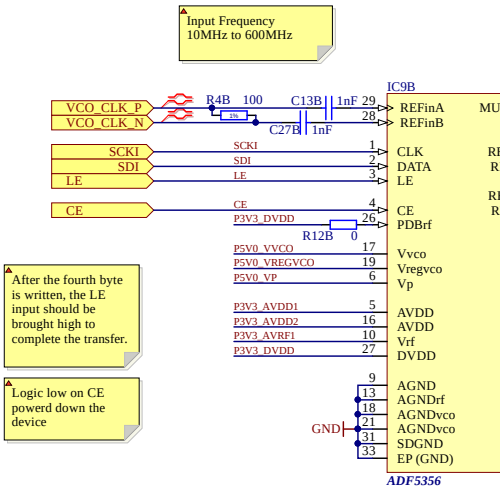
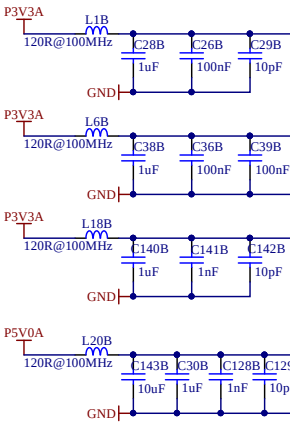
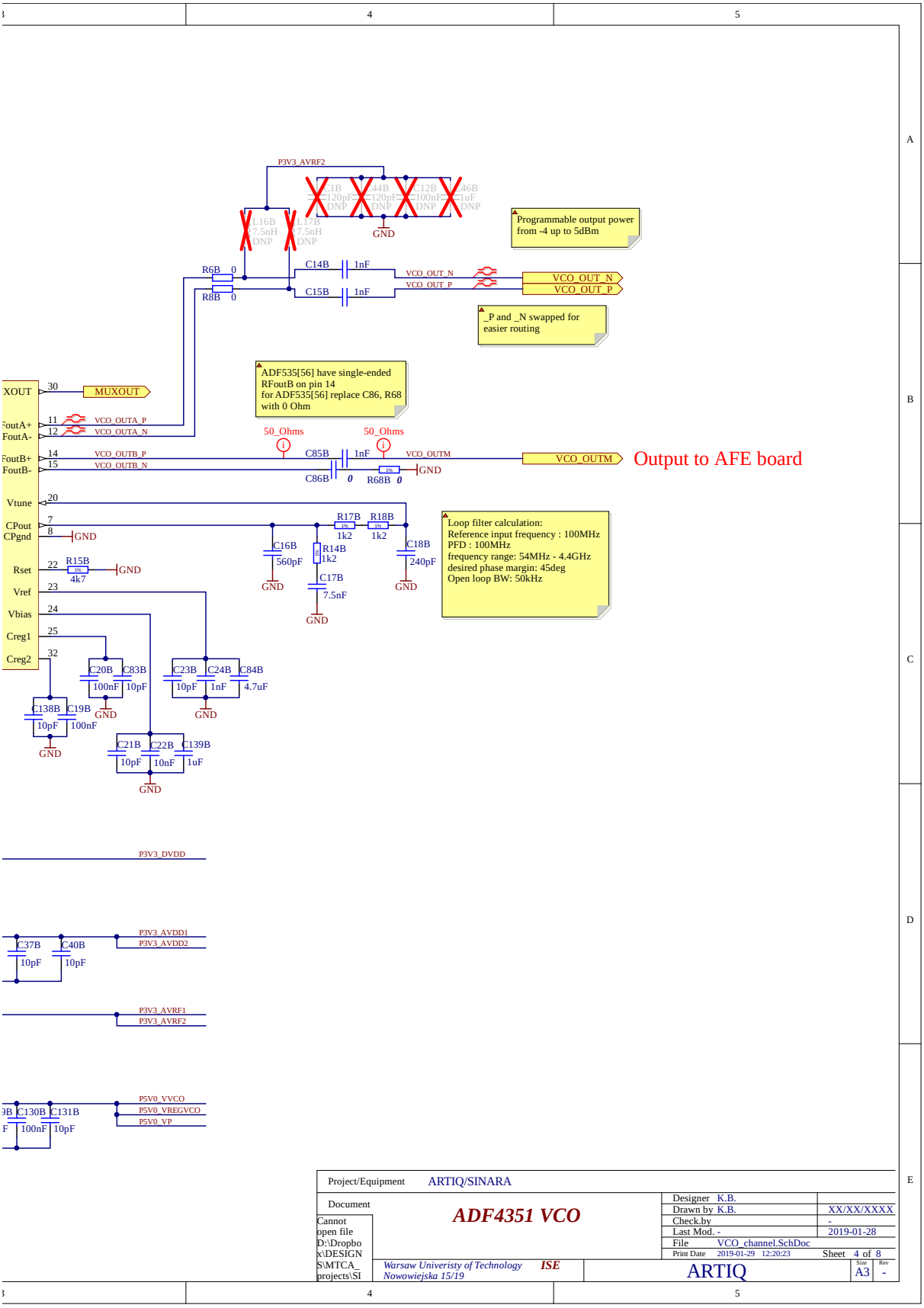


Figure 43. Loop Closed Before Output Divider

Start Freq	Stop Freq	VCO Divider	Channel Spacing
54.0MHz	106.25MHz	64	93.132uHz
106.25MHz	212.5MHz	32	186.26uHz
212.5MHz	425MHz	16	372.53uHz
425MHz	850MHz	8	745.06uHz
850MHz	1.70GHz	4	1.4901mHz
1.70GHz	3.40GHz	2	2.9802mHz
3.40GHz	4.40GHz	1	5.9605mHz






P3V3_AVRF2
C21B 120pF DNP
C44B 120pF DNP
C12B 100nF DNP
C46B 1uF DNP
GND
L16B 7.5nH DNP
L17B 7.5nH DNP
Programmable output power from -4 up to 5dBm
R6B 0
R8B 0
C14B 1nF
C15B 1nF
VCO_OUT_N
VCO_OUT_P
_P and _N swapped for easier routing
ADF535[56] have single-ended RFoutB on pin 14 for ADF535[56] replace C86, R68 with 0 Ohm
XOUT
30
MUXOUT
FoutA+
FoutA-
11
12
VCO_OUTA_P
VCO_OUTA_N
50_Ohms
50_Ohms
FoutB+
FoutB-
14
15
VCO_OUTB_P
VCO_OUTB_N
C85B 1nF
C86B 0
R68B 0
VCO_OUTM
Output to AFE board
Vtune
20
CPout
CPgnd
7
8
R17B 1k2
R18B 1k2
C16B 560pF
R14B 1k2
C17B 7.5nF
C18B 240pF
Loop filter calculation:
Reference input frequency : 100MHz
PFD : 100MHz
frequency range: 54MHz - 4.4GHz
desired phase margin: 45deg
Open loop BW: 50kHz
Rset
22
R15B 4k7
Vref
23
Vbias
24
Creg1
25
Creg2
32
C20B 100nF
C83B 10pF
C23B 10pF
C24B 1nF
C84B 4.7uF
C138B 10pF
C19B 100nF
C21B 10pF
C22B 10nF
C139B 1uF
P3V3_DVDD
C37B 10pF
C40B 10pF
P3V3_AVDD1
P3V3_AVDD2
P3V3_AVRF1
P3V3_AVRF2
C130B 100nF
C131B 10pF
P5V0_VVCO
P5V0_VREGVCO
P5V0_VP
Project/Equipment ARTIQ/SINARA
Document
ADF4351 VCO
Designer K.B.
Drawn by K.B.
XX/XX/XXXX
Check.by -
Last Mod. - 2019-01-28
File VCO_channel.SchDoc
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$$RF_{OUT} = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \times (f_{PFD})/RF\ Divider$$

where:

RF_{OUT} is the RF frequency output.
INT is the integer division factor.
$FRAC1$ is the fractionality.
$FRAC2$ is the auxiliary fractionality.
$MOD2$ is the auxiliary modulus.
$MOD1$ is the fixed 24-bit modulus.
RF Divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T)))$$

where:

REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
R is the RF reference division factor.
T is the reference divide by 2 bit (0 or 1).

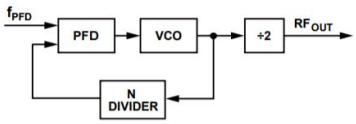

Figure 43. Loop Closed Before Output Divider

Start Freq	Stop Freq	VCO Divider	Channel Spacing
54.0MHz	106.25MHz	64	93.132uHz
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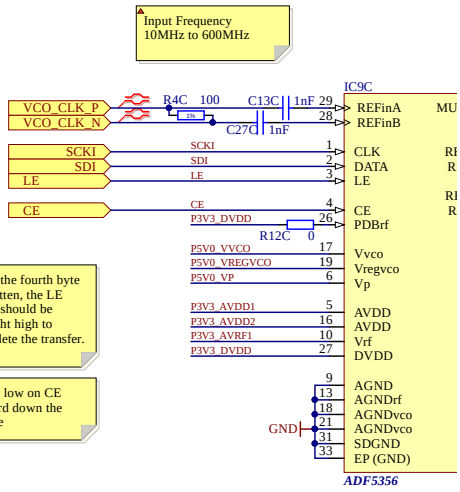
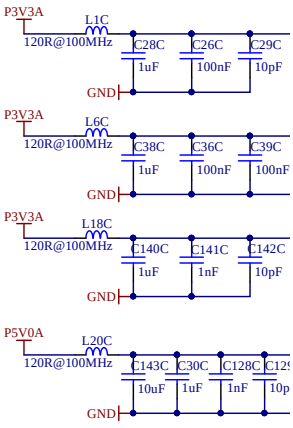
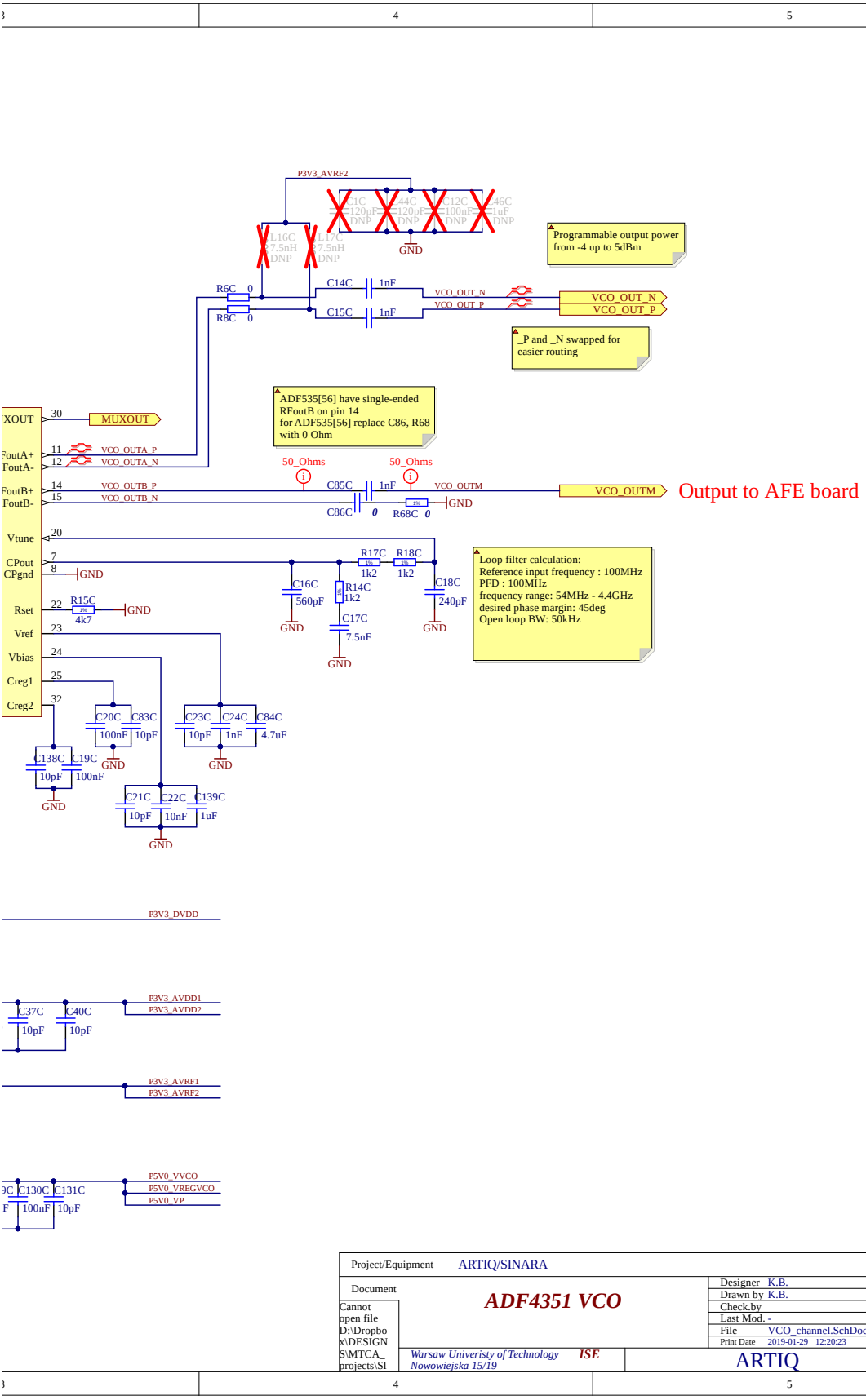
3.40GHz	4.40GHz	1	5.9605mHz






P3V3_AVRF2
C21C 120pF DNP
C44C 120pF DNP
C12C 100nF DNP
C46C 1uF DNP
GND
L16C 7.5nH DNP
L17C 7.5nH DNP
Programmable output power from -4 up to 5dBm
R6C 0
R8C 0
C14C 1nF
C15C 1nF
VCO_OUT_N
VCO_OUT_P
_P and _N swapped for easier routing
ADF535[56] have single-ended RFoutB on pin 14 for ADF535[56] replace C86, R68 with 0 Ohm
XOUT
30
MUXOUT
FoutA+
FoutA-
11
12
VCO_OUTA_P
VCO_OUTA_N
50_Ohms
50_Ohms
FoutB+
FoutB-
14
15
VCO_OUTB_P
VCO_OUTB_N
C85C 1nF
C86C 0
R68C 0
VCO_OUTM
Output to AFE board
Vtune
20
CPout
CPgnd
7
8
R17C 1k2
R18C 1k2
C16C 560pF
R14C 1k2
C17C 7.5nF
C18C 240pF
Loop filter calculation:
Reference input frequency : 100MHz
PFD : 100MHz
frequency range: 54MHz - 4.4GHz
desired phase margin: 45deg
Open loop BW: 50kHz
Rset
22
R15C 4k7
Vref
23
Vbias
24
Creg1
25
Creg2
32
C20C 100nF
C83C 10pF
C23C 10pF
C24C 1nF
C84C 4.7uF
C138C 10pF
C19C 100nF
C21C 10pF
C22C 10nF
C139C 1uF
P3V3_DVDD
P3V3_AVDD1
P3V3_AVDD2
C37C 10pF
C40C 10pF
P3V3_AVRF1
P3V3_AVRF2
P5V0_VVCO
P5V0_VREGVCO
P5V0_VP
C130C 100nF
C131C 10pF
Project/Equipment ARTIQ/SINARA
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ADF4351 VCO
Designer K.B.
Drawn by K.B.
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$$RF_{OUT} = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \times (f_{PFD})/RF\ Divider$$

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where:

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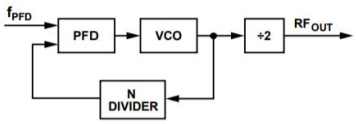

Figure 43. Loop Closed Before Output Divider

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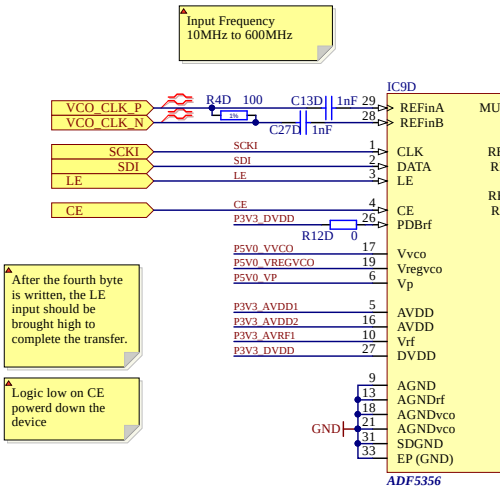

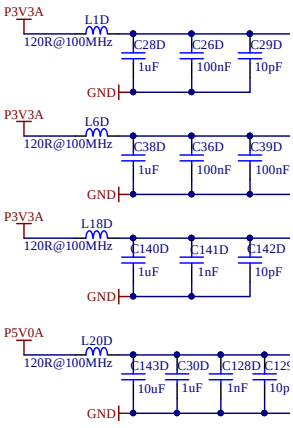

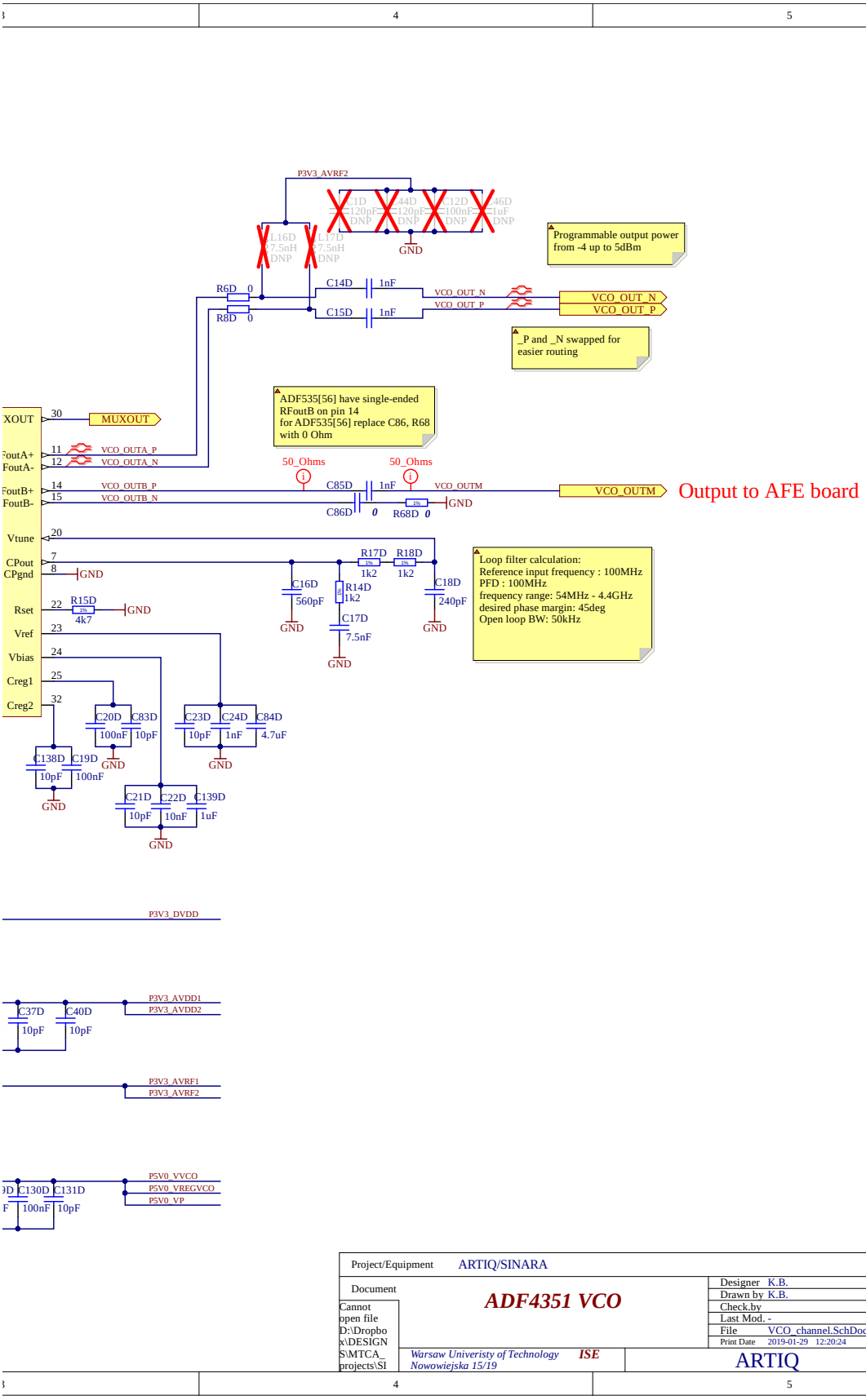
P3V3_AVRF2
C21D 120pF DNP
C44D 120pF DNP
C12D 100nF DNP
C46D 1uF DNP
GND
L16D 7.5nH DNP
L17D 7.5nH DNP
Programmable output power from -4 up to 5dBm
R6D 0
R8D 0
C14D 1nF
C15D 1nF
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XOUT
30
MUXOUT
FoutA+
FoutA-
11
12
VCO_OUTA_P
VCO_OUTA_N
50_Ohms
50_Ohms
FoutB+
FoutB-
14
15
VCO_OUTB_P
VCO_OUTB_N
C85D 1nF
C86D 0
R68D 0
VCO_OUTM
Output to AFE board
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7
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R17D 1k2
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R14D 1k2
C17D 7.5nF
C18D 240pF
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desired phase margin: 45deg
Open loop BW: 50kHz
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22
R15D 4k7
Vref
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Vbias
24
Creg1
25
Creg2
32
C20D 100nF
C83D 10pF
C23D 10pF
C24D 1nF
C84D 4.7uF
C138D 10pF
C19D 100nF
C21D 10pF
C22D 10nF
C139D 1uF
P3V3_DVDD
C37D 10pF
C40D 10pF
P3V3_AVDD1
P3V3_AVDD2
P3V3_AVRF1
P3V3_AVRF2
C130D 100nF
C131D 10pF
P5V0_VVCO
P5V0_VREGVCO
P5V0_VP
Project/Equipment ARTIQ/SINARA
Document
ADF4351 VCO
Designer K.B.
Drawn by K.B.
XX/XX/XXXX
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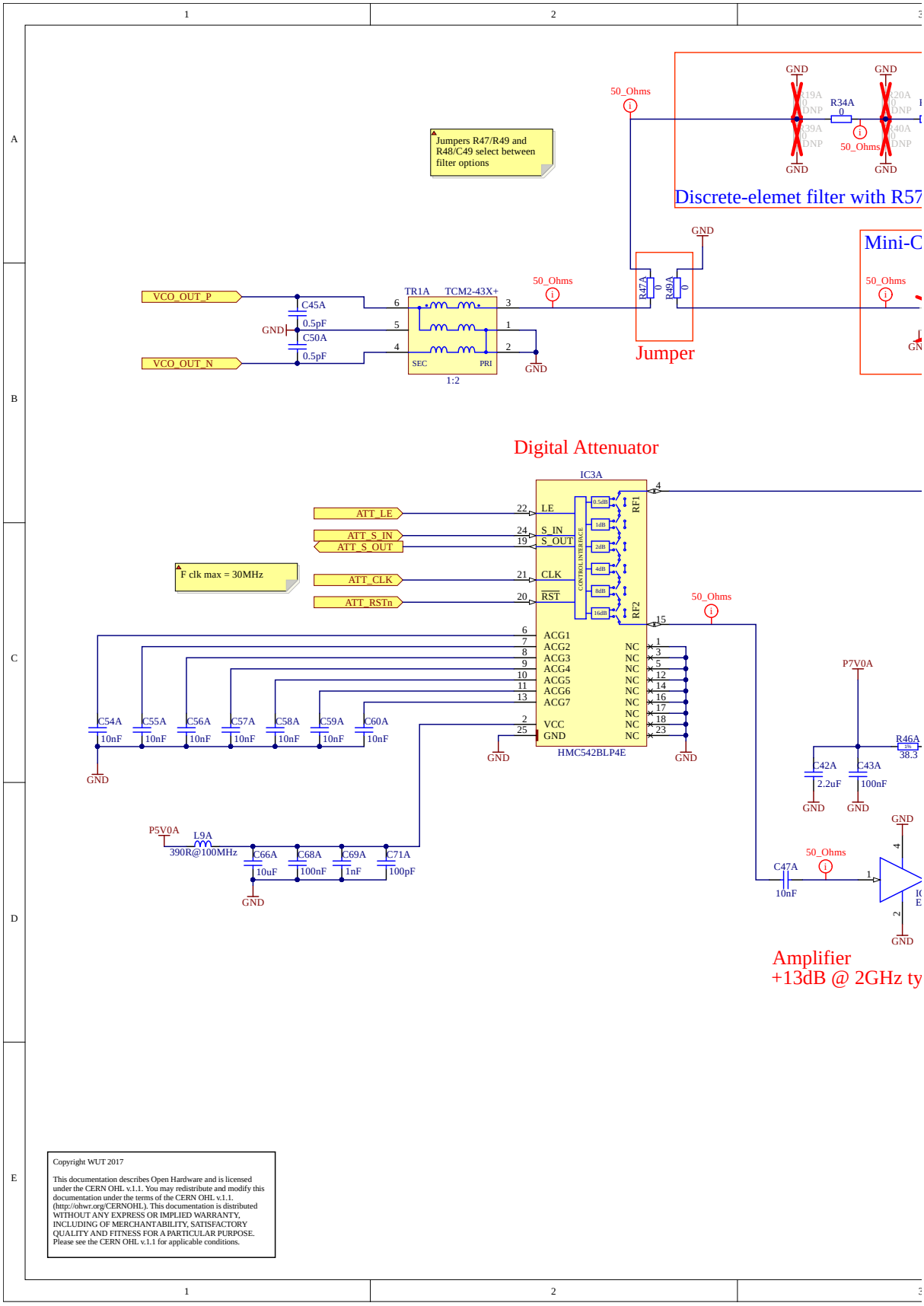
Jumpers R47/R49 and R48/C49 select between filter options
50_Ohms
GND
C19A 0 DNP
R34A 0
C20A 0 DNP
C39A 0 DNP
C40A 0 DNP
Discrete-elemet filter with R57
Mini-C
VCO_OUT_P
VCO_OUT_N
C45A 0.5pF
C50A 0.5pF
TR1A TCM2-43X+
SEC
PRI
1:2
R47A 0
R49A 0
Jumper
Digital Attenuator
IC3A
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
F clk max = 30MHz
LE
S_IN
S_OUT
CLK
RST
CONTROL INTERFACE
RF1
RF2
0.5dB
1dB
2dB
4dB
8dB
16dB
ACG1
ACG2
ACG3
ACG4
ACG5
ACG6
ACG7
VCC
NC
HMC542BLP4E
C54A 10nF
C55A 10nF
C56A 10nF
C57A 10nF
C58A 10nF
C59A 10nF
C60A 10nF
P5V0A
L9A 390R@100MHz
C66A 10uF
C68A 100nF
C69A 1nF
C71A 100pF
P7V0A
R46A 38.3
C42A 2.2uF
C43A 100nF
C47A 10nF
Amplifier
+13dB @ 2GHz ty
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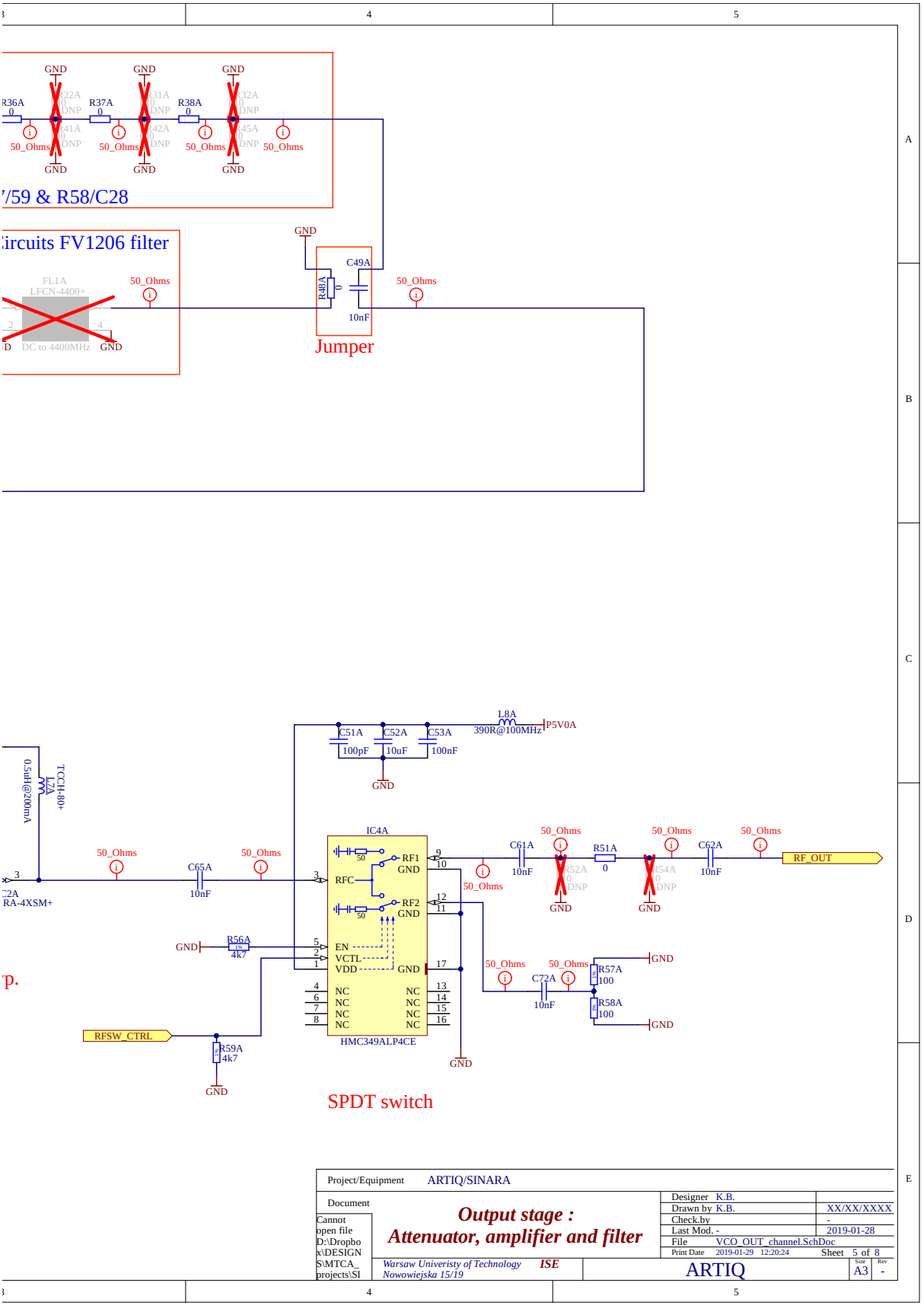
R36A
R37A
R38A
50_Ohms
GND
'/59 & R58/C28
ircuits FV1206 filter
FL1A
LFCN-4400+
DC to 4400MHz
C49A
10nF
Jumper
L8A
390R@100MHz
P5V0A
C51A
100pF
C52A
10uF
C53A
100nF
0.5uH@200mA
TCCH-80+
RA-4XSM+
C65A
10nF
IC4A
RF1
RF2
RFC
EN
VCTL
VDD
NC
HMC349ALP4CE
R56A
4k7
RFSW_CTRL
R59A
4k7
C61A
10nF
R51A
0
C62A
10nF
RF_OUT
R57A
100
R58A
100
C72A
10nF
SPDT switch
Project/Equipment ARTIQ/SINARA
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Attenuator, amplifier and filter
Designer K.B.
Drawn by K.B.
XX/XX/XXXX
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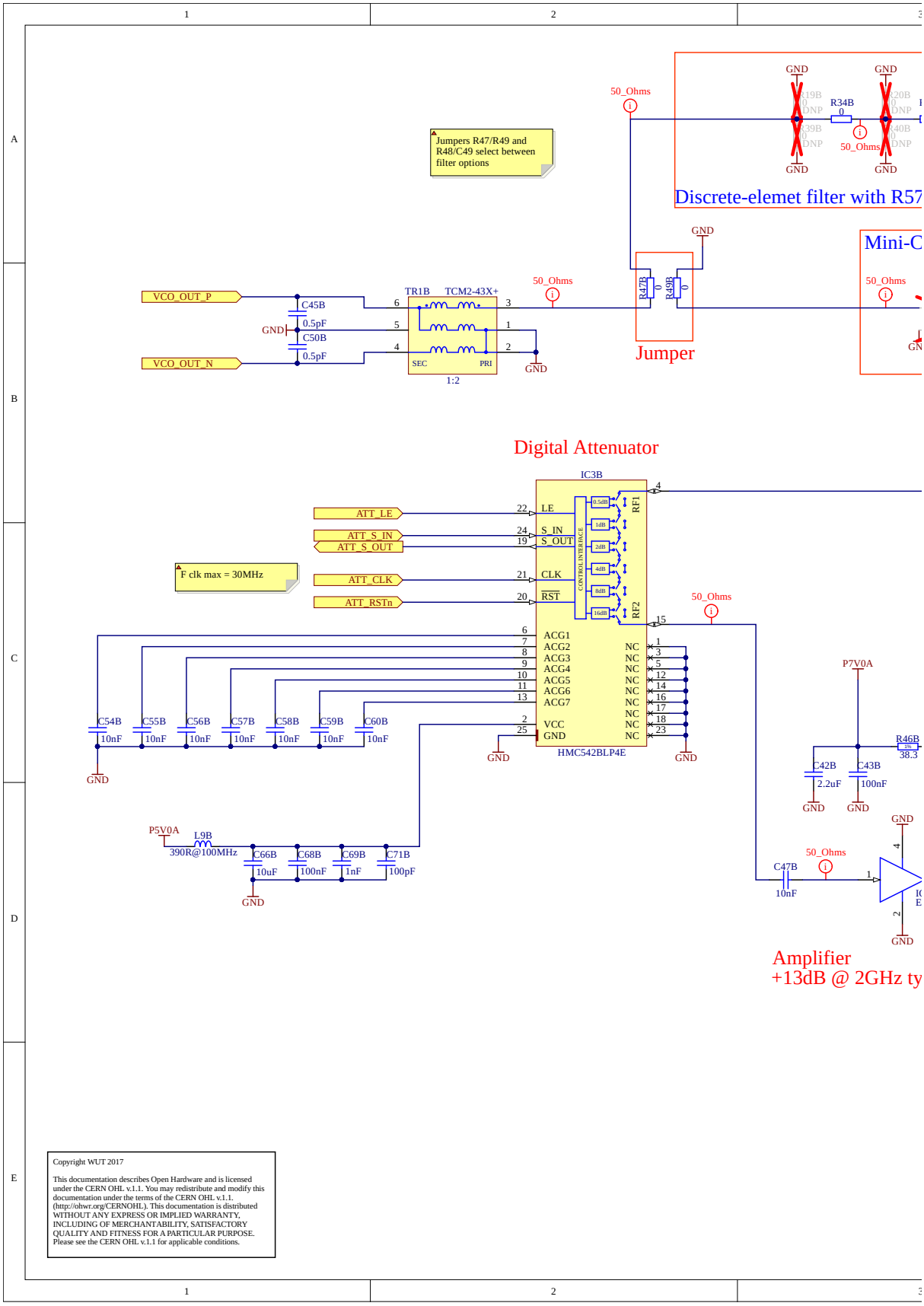

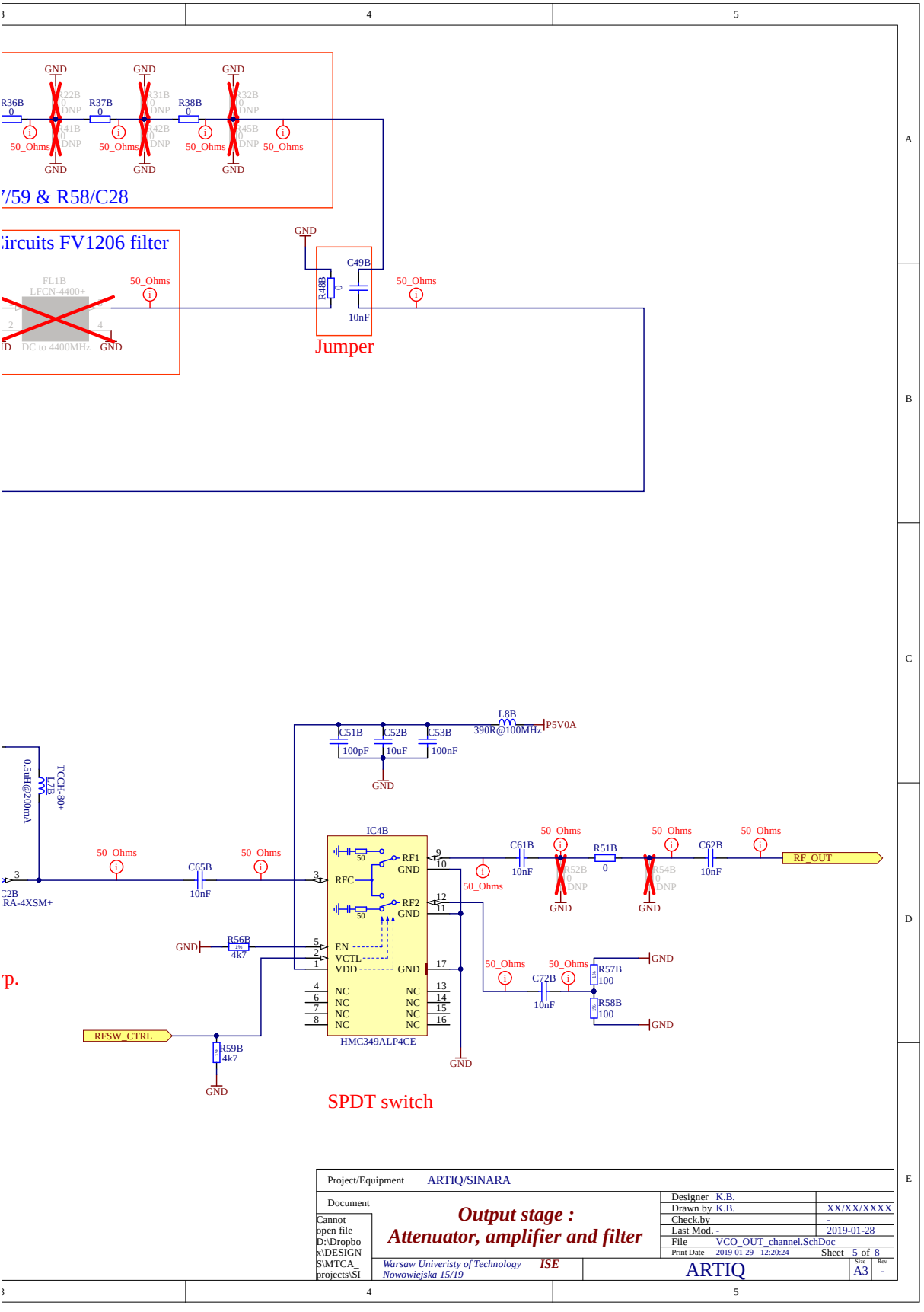
GND
R36B
0
R37B
0
R38B
0
50_Ohms
'/59 & R58/C28
ircuits FV1206 filter
FL1B
LFCN-4400+
DC to 4400MHz
R48B
C49B
10nF
Jumper
L8B
390R@100MHz
P5V0A
C51B
100pF
C52B
10uF
C53B
100nF
0.5uH@200mA
TCCH-80+
RA-4XSM+
C65B
10nF
IC4B
RF1
RF2
RFC
EN
VCTL
VDD
NC
HMC349ALP4CE
C61B
10nF
R51B
0
C62B
10nF
RF_OUT
R56B
4k7
RFSW_CTRL
R59B
4k7
C72B
10nF
R57B
100
R58B
100
SPDT switch
Project/Equipment ARTIQ/SINARA
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Attenuator, amplifier and filter
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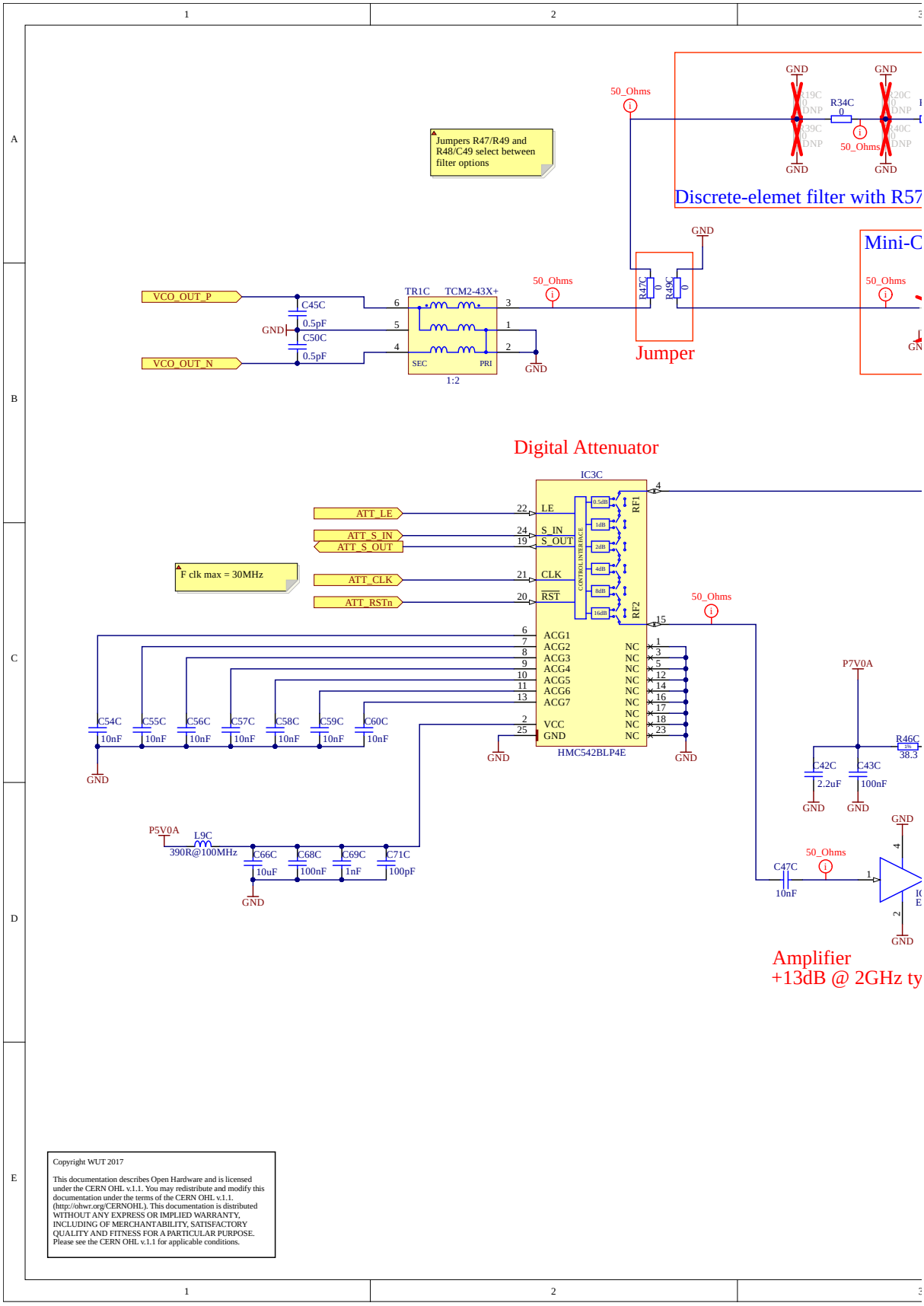

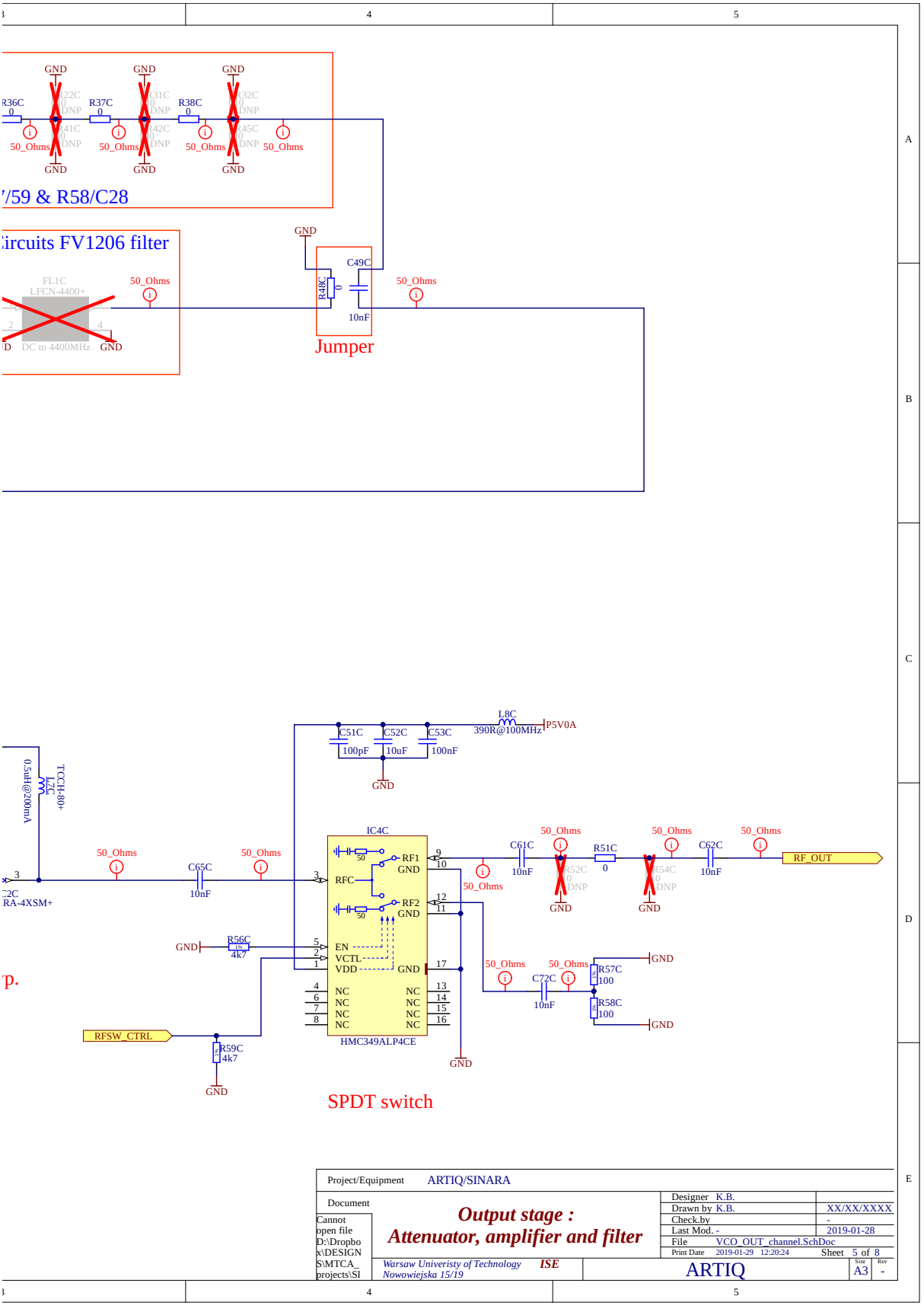
GND
R36C
0
50_Ohms
R37C
0
R38C
0
'/59 & R58/C28
ircuits FV1206 filter
FL1C
LFCN-4400+
DC to 4400MHz
C49C
R48C
10nF
Jumper
L8C
390R@100MHz
P5V0A
C51C
100pF
C52C
10uF
C53C
100nF
0.5uH@200mA
TCCH-80+
IC4C
RF1
RF2
RFC
EN
VCTL
VDD
NC
HMC349ALP4CE
C65C
10nF
R56C
4k7
RFSW_CTRL
R59C
4k7
C61C
10nF
R51C
0
C62C
10nF
RF_OUT
C72C
10nF
R57C
100
R58C
100
SPDT switch
Project/Equipment ARTIQ/SINARA
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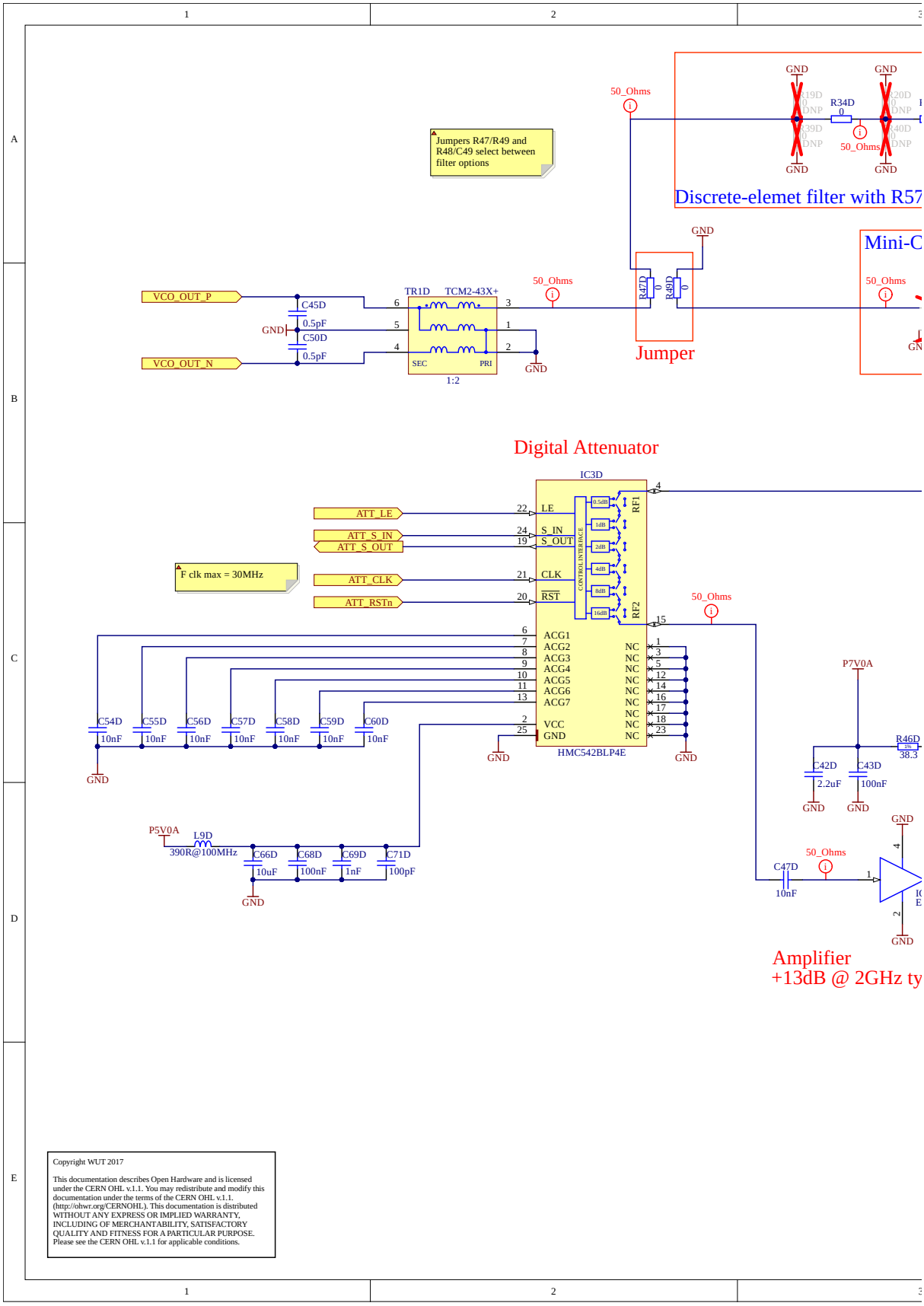
Jumpers R47/R49 and R48/C49 select between filter options
Discrete-elemet filter with R57
Mini-C
Jumper
Digital Attenuator
Amplifier
+13dB @ 2GHz ty
IC3D
HMC542BLP4E
TR1D TCM2-43X+
1:2
F clk max = 30MHz
VCO_OUT_P
VCO_OUT_N
ATT_LE
ATT_S_IN
ATT_S_OUT
ATT_CLK
ATT_RSTn
50_Ohms
GND
P5V0A
P7V0A
L9D
390R@100MHz
R34D
R46D
R47D
R49D
C45D
C50D
C54D
C55D
C56D
C57D
C58D
C59D
C60D
C66D
C68D
C69D
C71D
C42D
C43D
C47D
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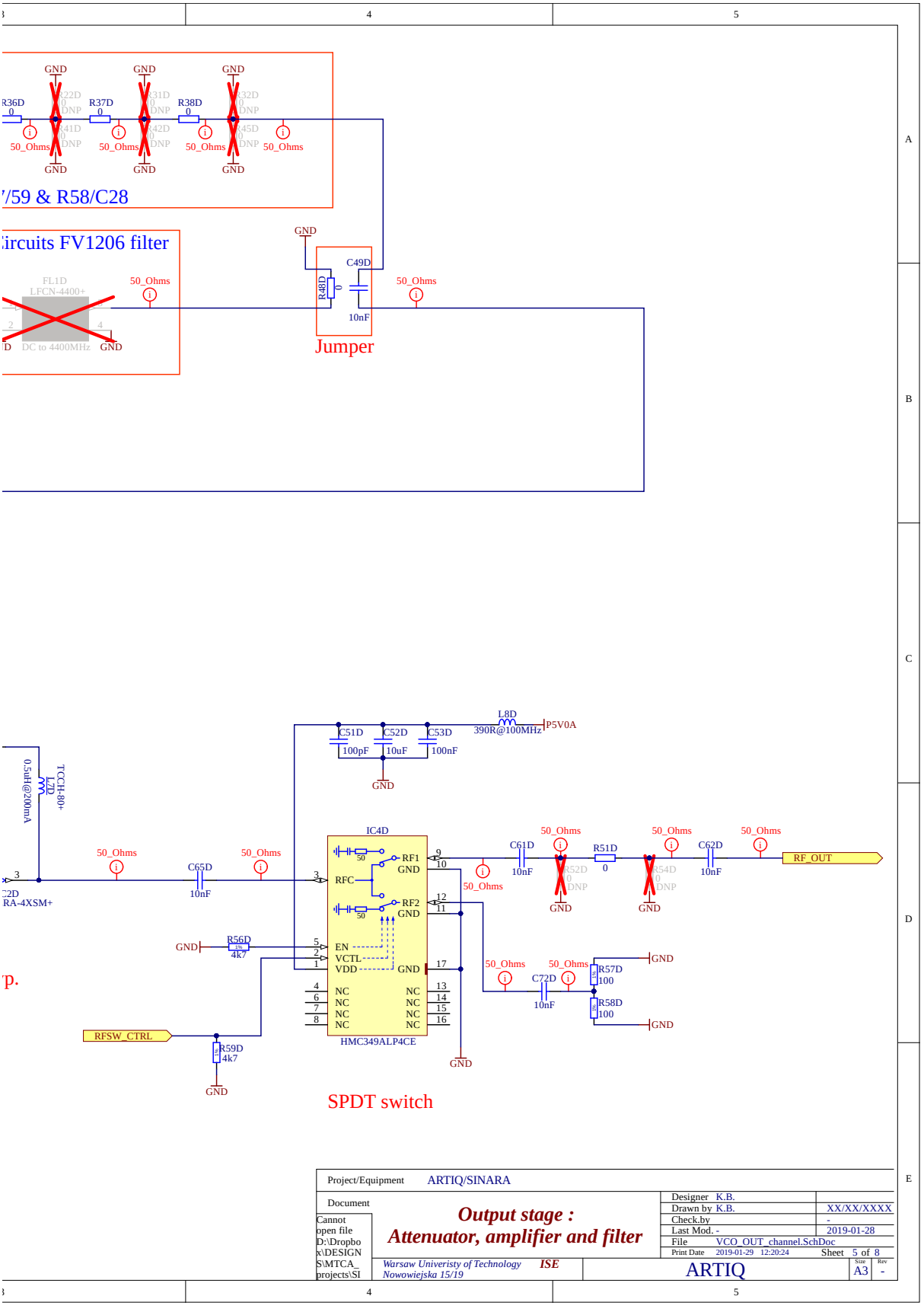
GND
R36D
0
R37D
0
R38D
0
50_Ohms
/59 & R58/C28
ircuits FV1206 filter
FL1D
LFCN-4400+
DC to 4400MHz
C49D
R48D
10nF
Jumper
L8D
390R@100MHz
P5V0A
C51D
100pF
C52D
10uF
C53D
100nF
0.5uH@200mA
TCCH-80+
RA-4XSM+
C65D
10nF
IC4D
RF1
RF2
RFC
EN
VCTL
VDD
NC
HMC349ALP4CE
C61D
10nF
R51D
0
C62D
10nF
RF_OUT
R56D
4k7
RFSW_CTRL
R59D
4k7
C72D
10nF
R57D
100
R58D
100
SPDT switch
Project/Equipment ARTIQ/SINARA
Document
Cannot open file D:\Dropbox\DESIGNS\MTCA_projects\SI
Output stage :
Attenuator, amplifier and filter
Designer K.B.
Drawn by K.B.
XX/XX/XXXX
Check.by -
Last Mod. - 2019-01-28
File VCO_OUT_channel.SchDoc
Print Date 2019-01-29 12:20:24
Sheet 5 of 8
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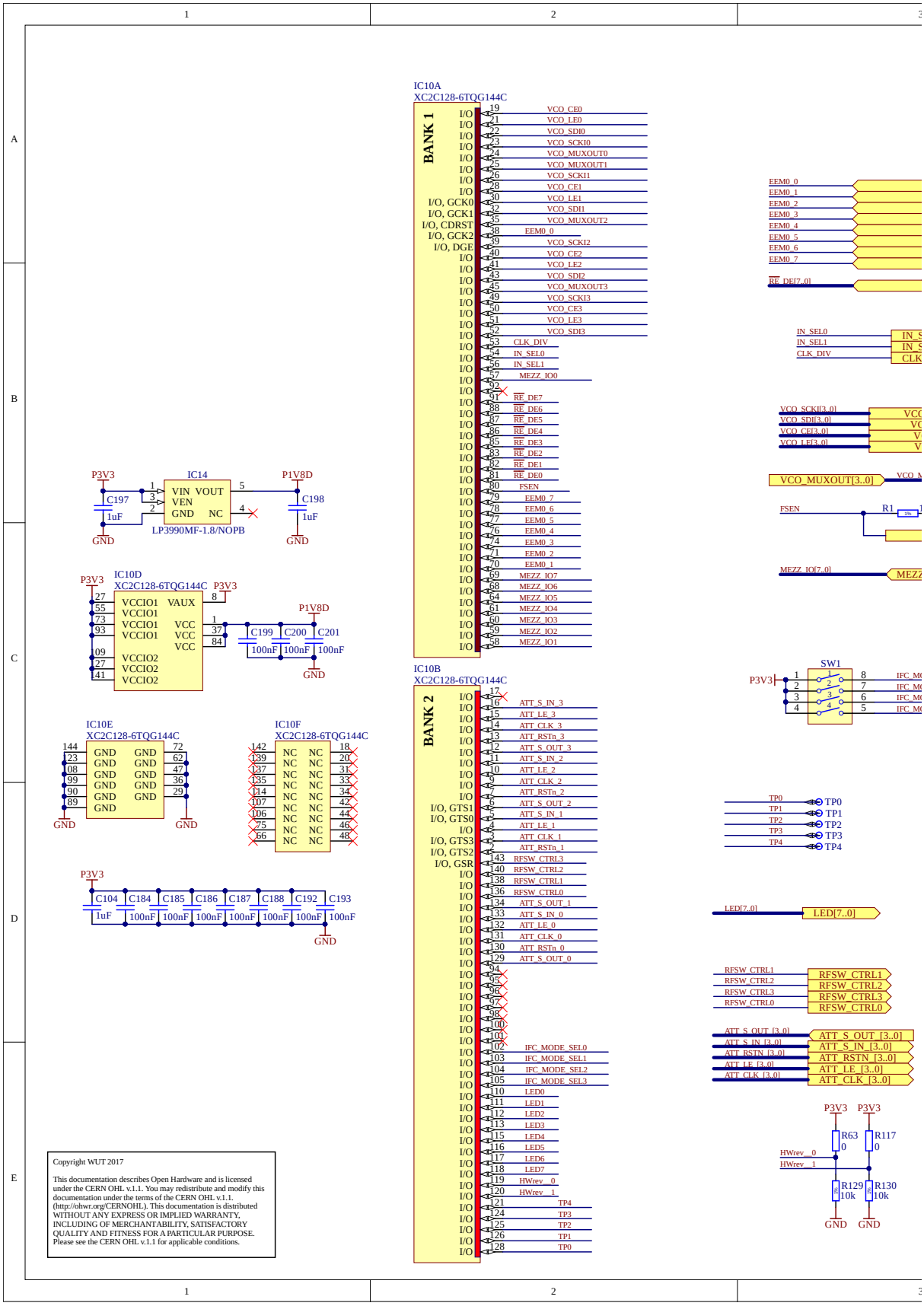
ARTIQ
Size A3
Rev -


IC10A
XC2C128-6TQG144C
BANK 1
IC10B
XC2C128-6TQG144C
BANK 2
IC14
LP3990MF-1.8/NOPB
IC10D
XC2C128-6TQG144C
IC10E
XC2C128-6TQG144C
IC10F
XC2C128-6TQG144C
SW1
P3V3
P1V8D
GND
VCO_CE0
VCO_LE0
VCO_SDI0
VCO_SCKI0
VCO_MUXOUT0
VCO_MUXOUT1
VCO_SCKI1
VCO_CE1
VCO_LE1
VCO_SDI1
VCO_MUXOUT2
EEM0_0
VCO_SCKI2
VCO_CE2
VCO_LE2
VCO_SDI2
VCO_MUXOUT3
VCO_SCKI3
VCO_CE3
VCO_LE3
VCO_SDI3
CLK_DIV
IN_SEL0
IN_SEL1
MEZZ_IO0
RE_DE7
RE_DE6
RE_DE5
RE_DE4
RE_DE3
RE_DE2
RE_DE1
RE_DE0
FSEN
EEM0_7
EEM0_6
EEM0_5
EEM0_4
EEM0_3
EEM0_2
EEM0_1
MEZZ_IO7
MEZZ_IO6
MEZZ_IO5
MEZZ_IO4
MEZZ_IO3
MEZZ_IO2
MEZZ_IO1
ATT_S_IN_3
ATT_LE_3
ATT_CLK_3
ATT_RSTn_3
ATT_S_OUT_3
ATT_S_IN_2
ATT_LE_2
ATT_CLK_2
ATT_RSTn_2
ATT_S_OUT_2
ATT_S_IN_1
ATT_LE_1
ATT_CLK_1
ATT_RSTn_1
RFSW_CTRL3
RFSW_CTRL2
RFSW_CTRL1
RFSW_CTRL0
ATT_S_OUT_1
ATT_S_IN_0
ATT_LE_0
ATT_CLK_0
ATT_RSTn_0
ATT_S_OUT_0
IFC_MODE_SEL0
IFC_MODE_SEL1
IFC_MODE_SEL2
IFC_MODE_SEL3
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
HWrev__0
HWrev__1
TP4
TP3
TP2
TP1
TP0
EEM0_0
EEM0_1
EEM0_2
EEM0_3
EEM0_4
EEM0_5
EEM0_6
EEM0_7
RE_DE[7..0]
IN_SEL0
IN_SEL1
CLK_DIV
VCO_SCKI[3..0]
VCO_SDI[3..0]
VCO_CE[3..0]
VCO_LE[3..0]
VCO_MUXOUT[3..0]
FSEN
MEZZ_IO[7..0]
TP0
TP1
TP2
TP3
TP4
LED[7..0]
RFSW_CTRL1
RFSW_CTRL2
RFSW_CTRL3
RFSW_CTRL0
ATT_S_OUT_[3..0]
ATT_S_IN_[3..0]
ATT_RSTN_[3..0]
ATT_LE_[3..0]
ATT_CLK_[3..0]
R63
R117
R129
R130
10k
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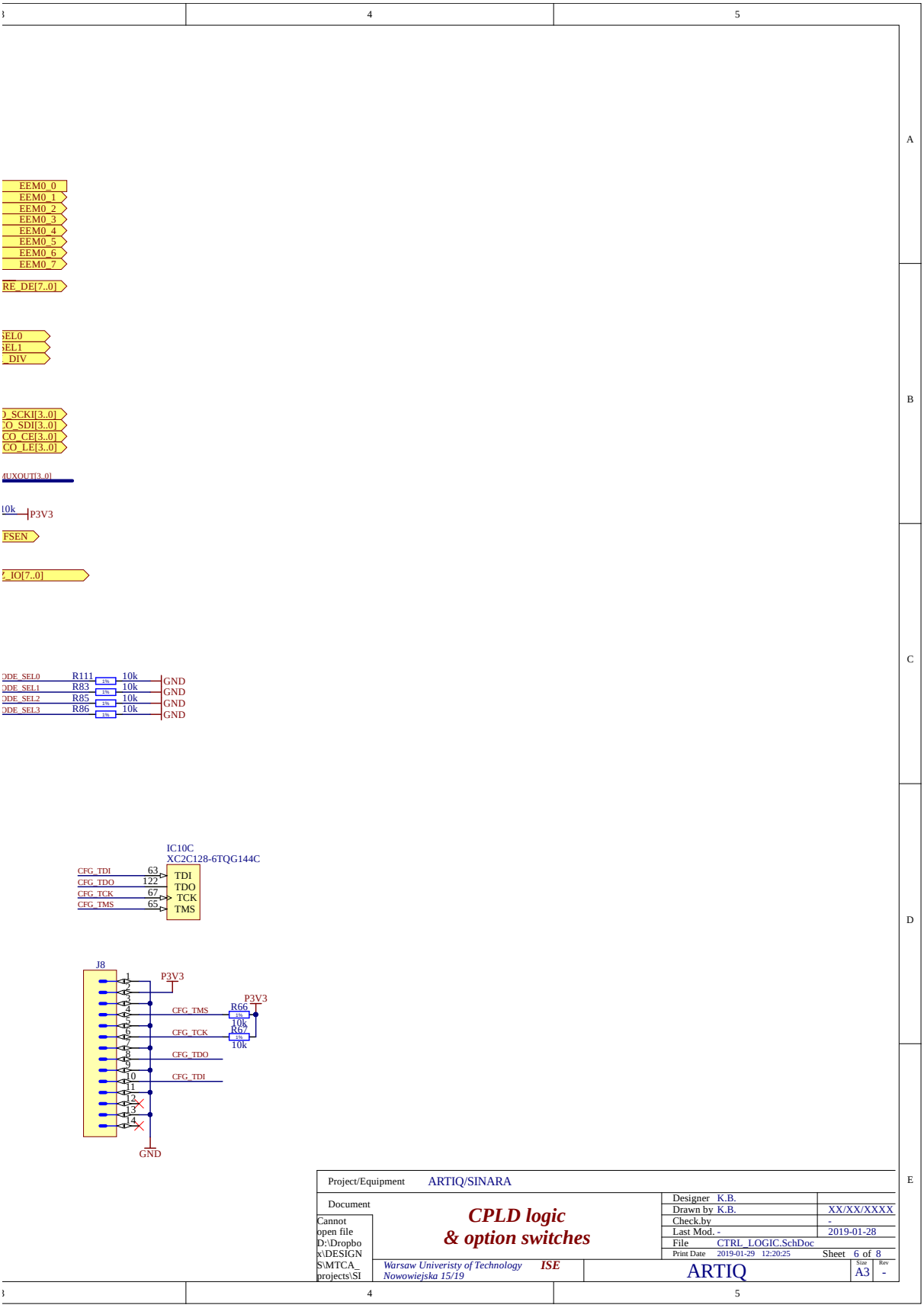
EEM0_0
EEM0_1
EEM0_2
EEM0_3
EEM0_4
EEM0_5
EEM0_6
EEM0_7
RE_DE[7..0]
EL0
EL1
_DIV
_SCKI[3..0]
O_SDI[3..0]
CO_CE[3..0]
CO_LE[3..0]
UXOUT[3..0]
10k
P3V3
FSEN
_IO[7..0]
DE_SEL0
DE_SEL1
DE_SEL2
DE_SEL3
R111
R83
R85
R86
10k
1%
GND
IC10C
XC2C128-6TQG144C
CFG_TDI
CFG_TDO
CFG_TCK
CFG_TMS
63
122
67
65
TDI
TDO
TCK
TMS
J8
R66
R67
Project/Equipment
ARTIQ/SINARA
Document
CPLD logic
& option switches
Cannot
open file
D:\Dropbo
x\DESIGN
S\MTCA_
projects\SI
Designer K.B.
Drawn by K.B.
XX/XX/XXXX
Check.by
-
Last Mod. -
2019-01-28
File CTRL_LOGIC.SchDoc
Print Date 2019-01-29 12:20:25
Sheet 6 of 8
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ARTIQ
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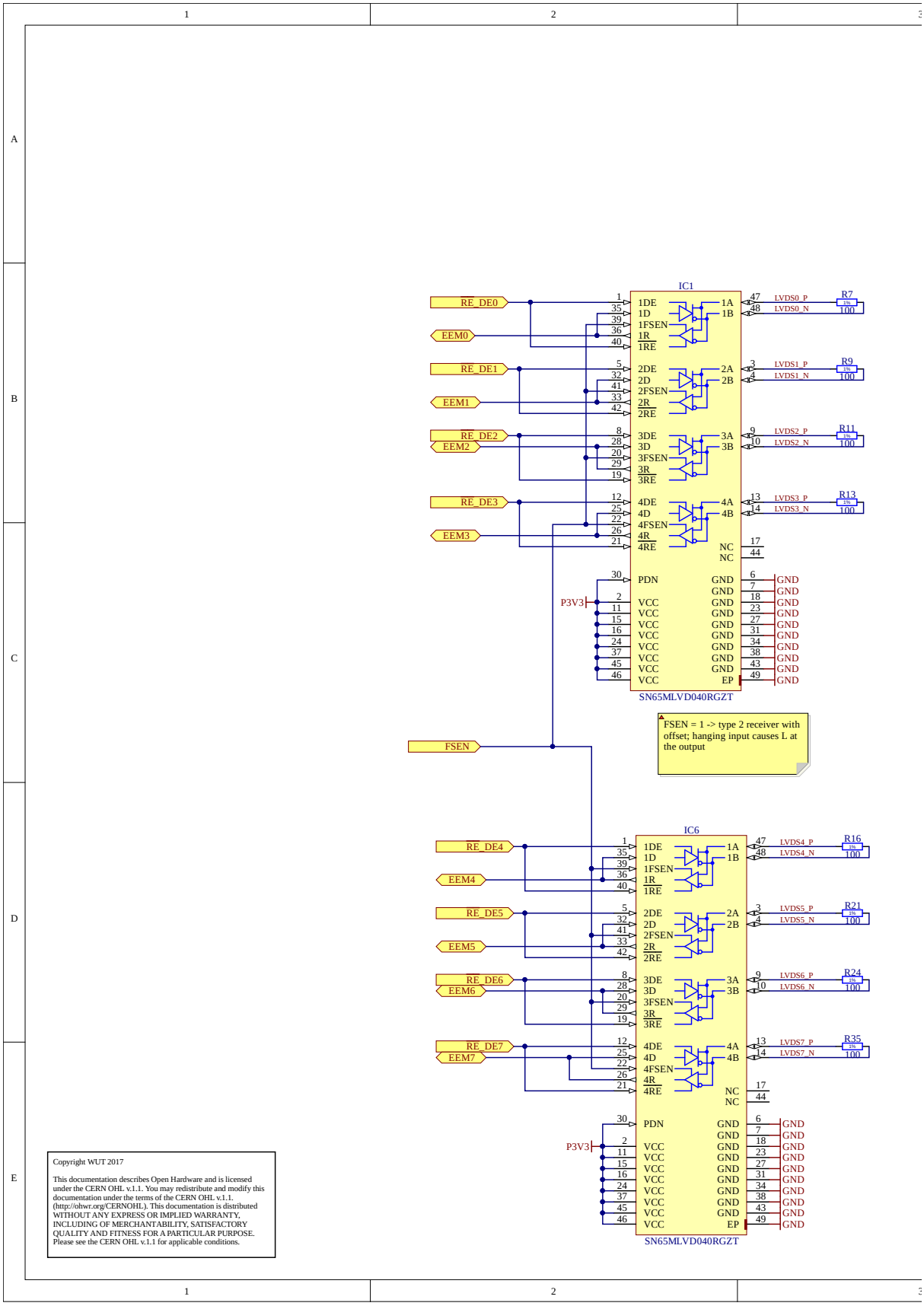
Rev -


IC1
RE_DE0
EEM0
RE_DE1
EEM1
RE_DE2
EEM2
RE_DE3
EEM3
1DE
1D
1FSEN
1R
1RE
2DE
2D
2FSEN
2R
2RE
3DE
3D
3FSEN
3R
3RE
4DE
4D
4FSEN
4R
4RE
1A
1B
2A
2B
3A
3B
4A
4B
NC
PDN
VCC
GND
EP
P3V3
LVDS0_P
LVDS0_N
LVDS1_P
LVDS1_N
LVDS2_P
LVDS2_N
LVDS3_P
LVDS3_N
R7
R9
R11
R13
100
SN65MLVD040RGZT
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output
FSEN
IC6
RE_DE4
EEM4
RE_DE5
EEM5
RE_DE6
EEM6
RE_DE7
EEM7
LVDS4_P
LVDS4_N
LVDS5_P
LVDS5_N
LVDS6_P
LVDS6_N
LVDS7_P
LVDS7_N
R16
R21
R24
R35
SN65MLVD040RGZT
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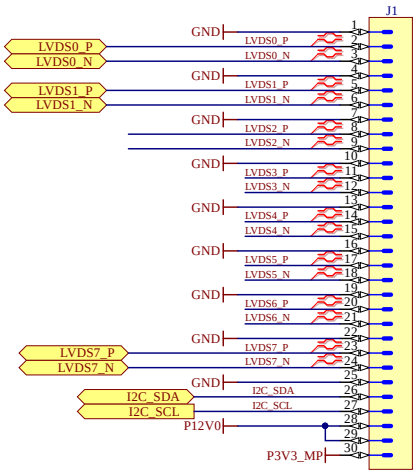
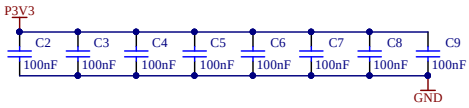
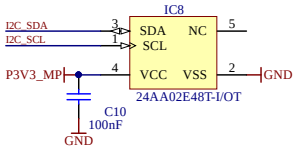
EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A







Project/Equipment	ARTIQ/SINARA		
Document	***LVDS to LVTTL interface & EEM connector***	Designer K.B.	
		Drawn by K.B.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	2018-11-15
Cannot open file D:\Dropbox\DESIGNS\MTCA_projects\SI		File LVDS_IFC_VCO.SchDoc	
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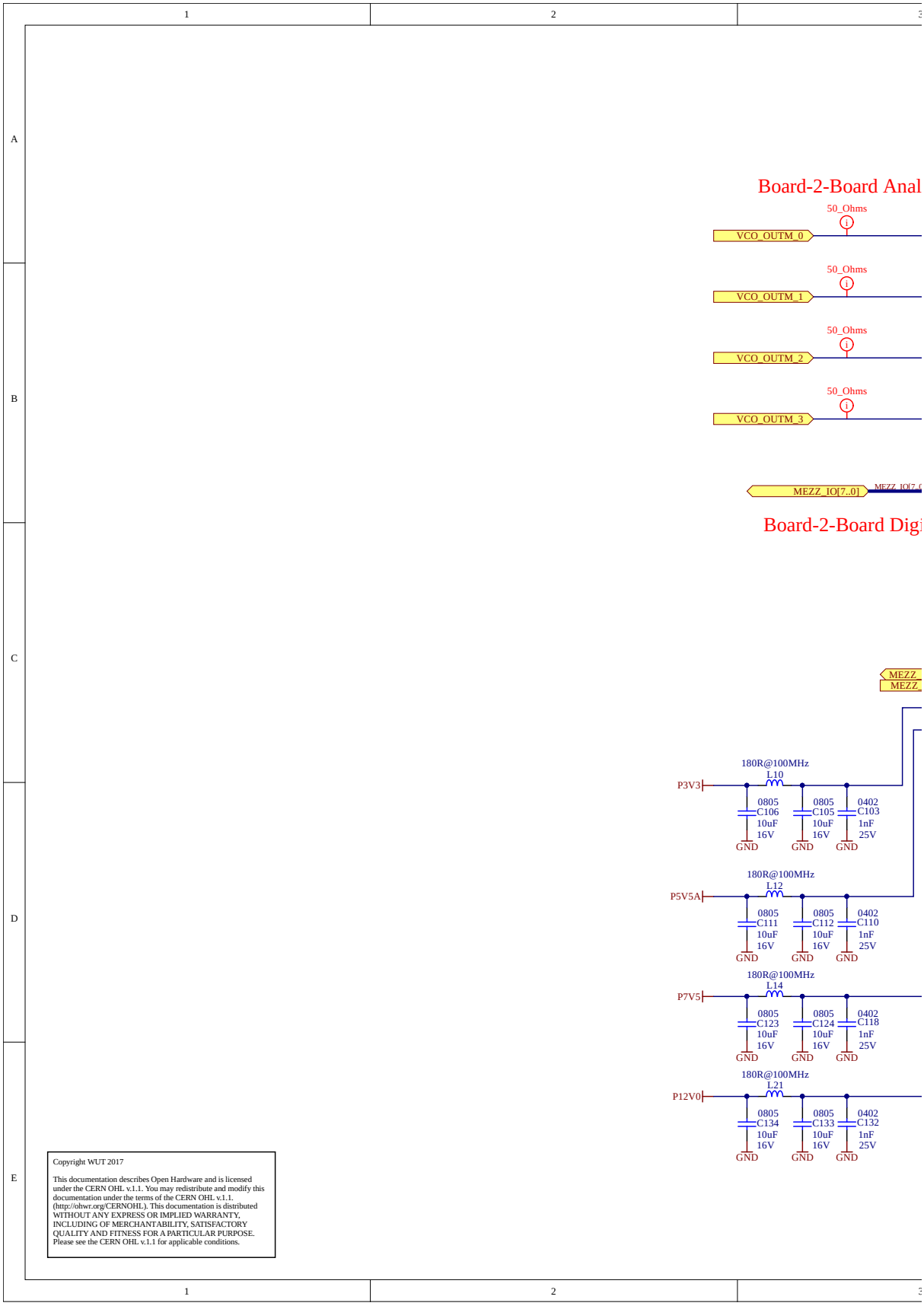
Warsaw Univeristy of Technology ***ISE*** *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -


1
2
3
A
B
C
D
E
Board-2-Board Anal
50_Ohms
VCO_OUTM_0
50_Ohms
VCO_OUTM_1
50_Ohms
VCO_OUTM_2
50_Ohms
VCO_OUTM_3
MEZZ_IO[7..0]
Board-2-Board Digi
MEZZ
MEZZ
180R@100MHz
L10
P3V3
0805
C106
10uF
16V
GND
0805
C105
10uF
16V
GND
0402
C103
1nF
25V
GND
180R@100MHz
L12
P5V5A
0805
C111
10uF
16V
GND
0805
C112
10uF
16V
GND
0402
C110
1nF
25V
GND
180R@100MHz
L14
P7V5
0805
C123
10uF
16V
GND
0805
C124
10uF
16V
GND
0402
C118
1nF
25V
GND
180R@100MHz
L21
P12V0
0805
C134
10uF
16V
GND
0805
C133
10uF
16V
GND
0402
C132
1nF
25V
GND
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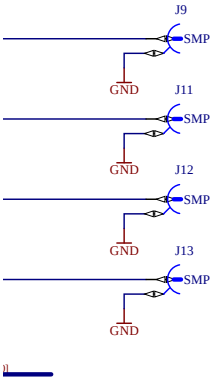
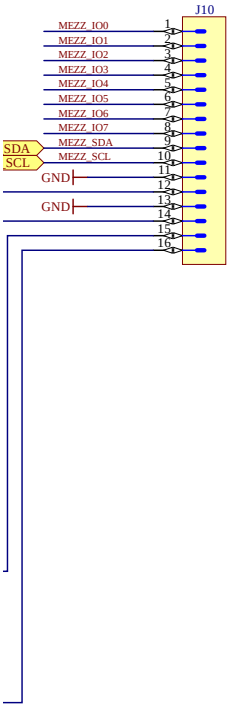
og Connectors



ital Connectors



Project/Equipment	ARTIQ/SINARA		
Document	**AFE Mezzanine Connectors**	Designer K.B.	
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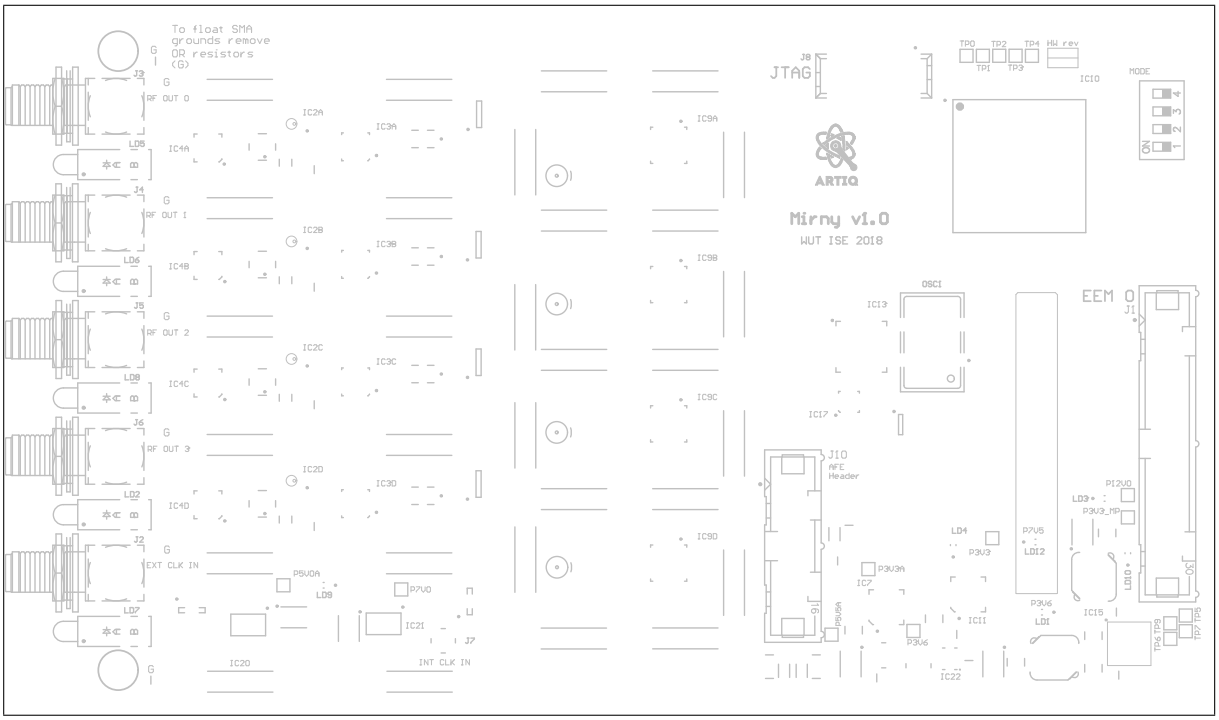
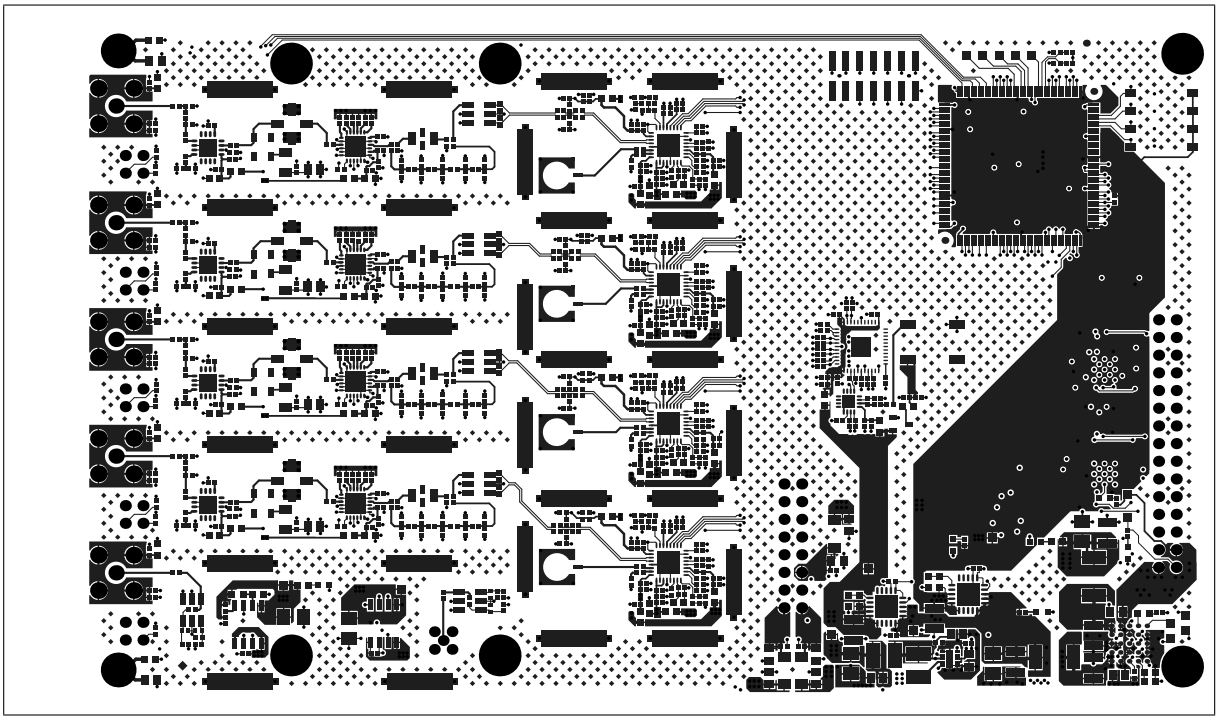
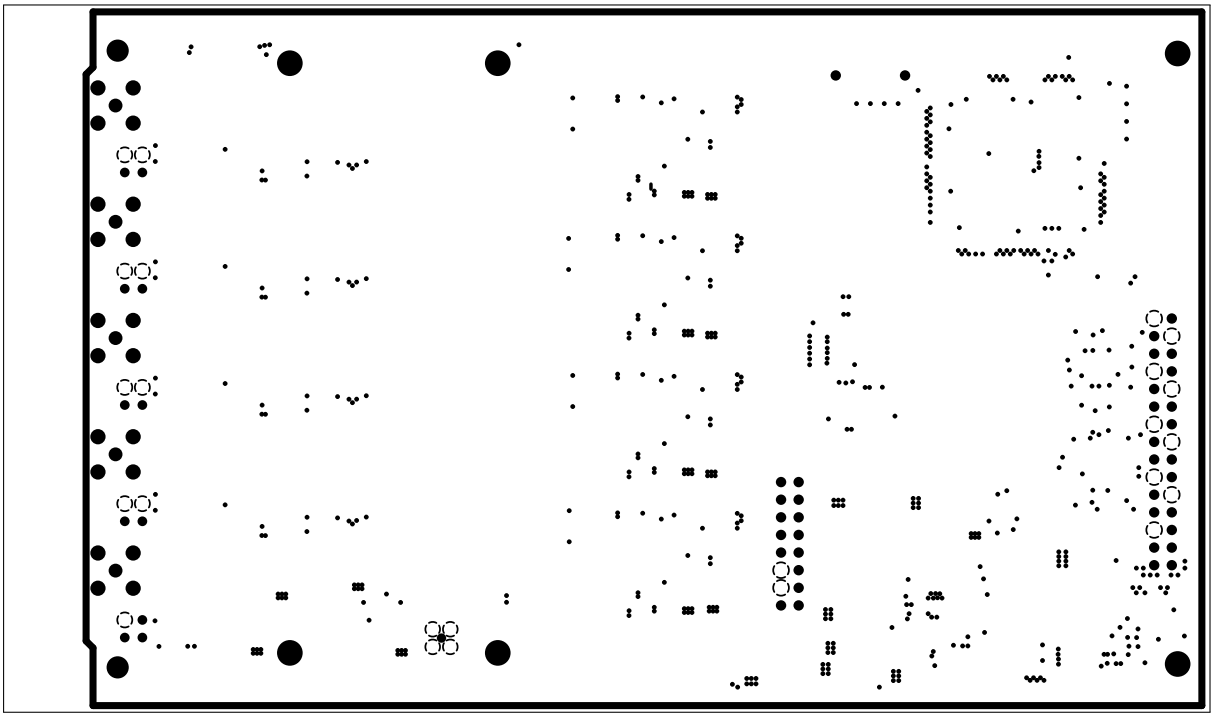
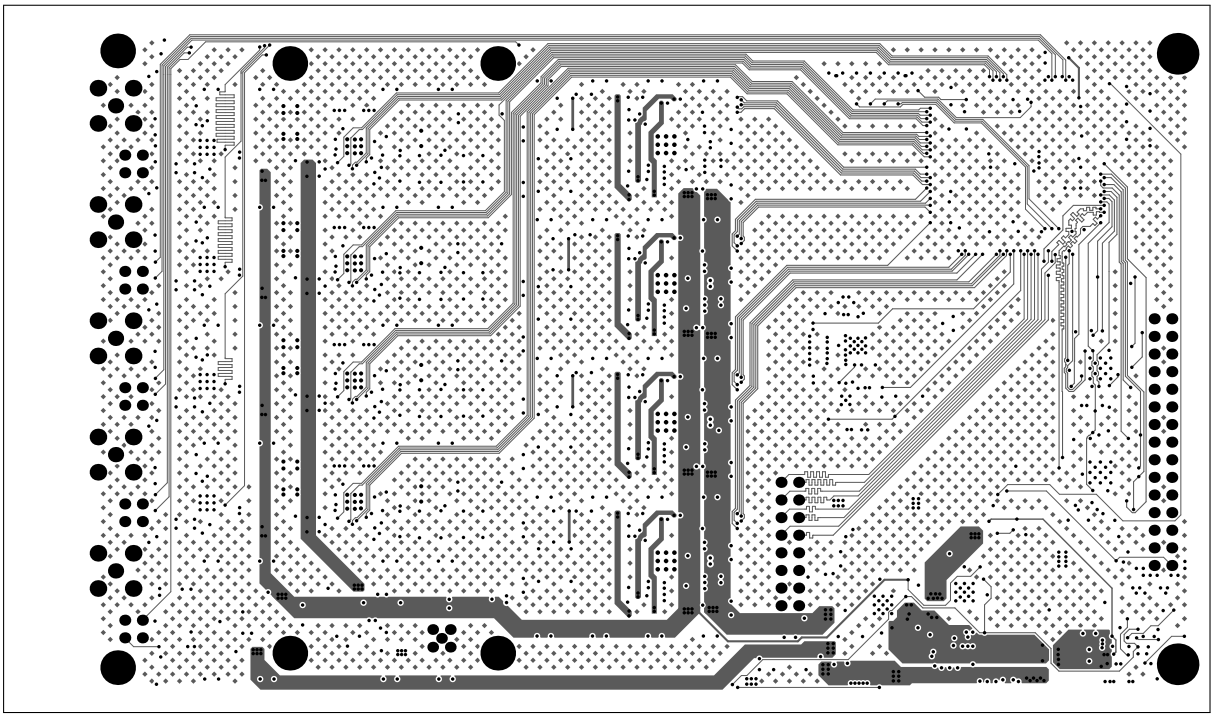
		Last Mod. -	2019-01-28
		File B2B_connectors.SchDoc	
		Print Date 2019-01-29 12:20:25	Sheet 8 of 8
Warsaw Univeristy of Technology **ISE** *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -

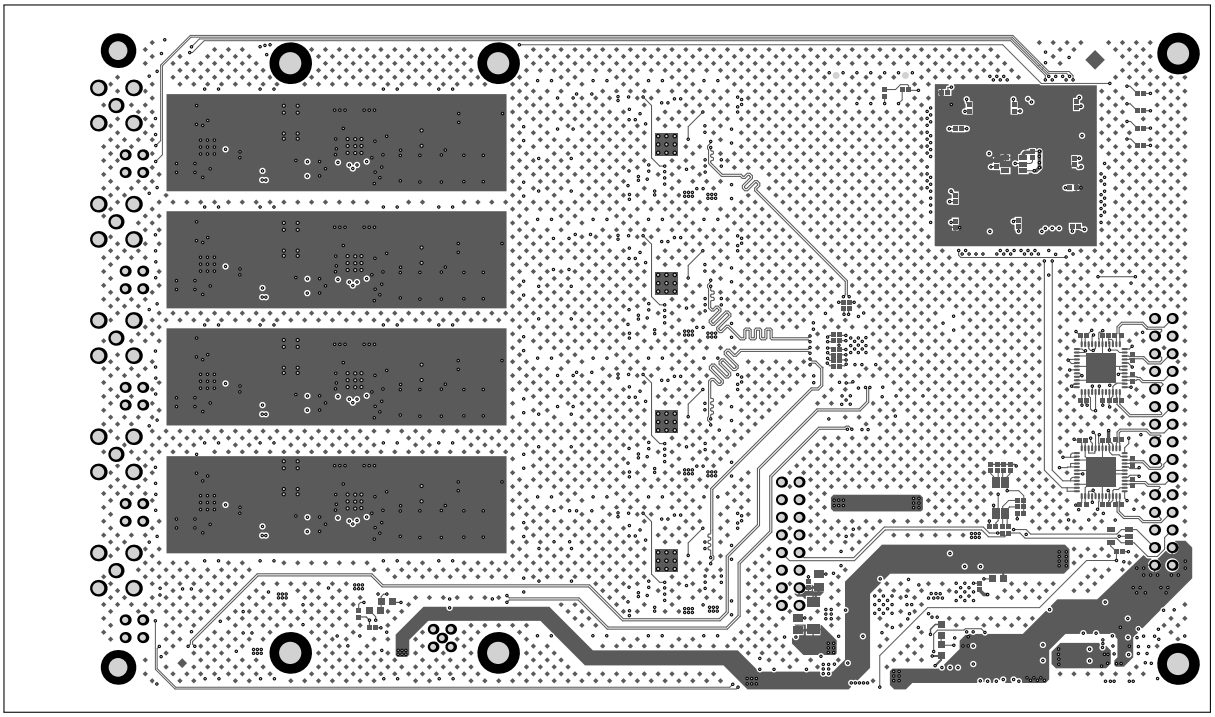
8.2 Appendix B - PCB gerber masks











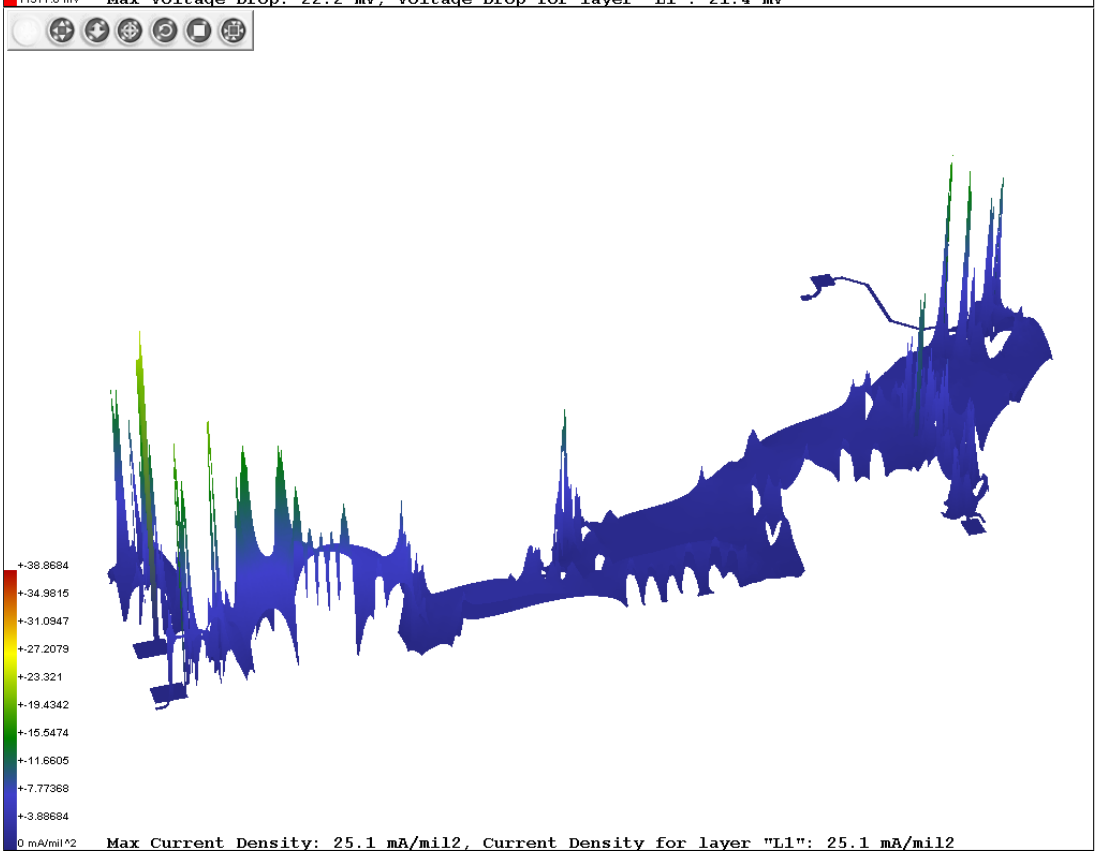

ARTIQ
Mirny v1.0

8.3 Appendix C - PCB layer stackup

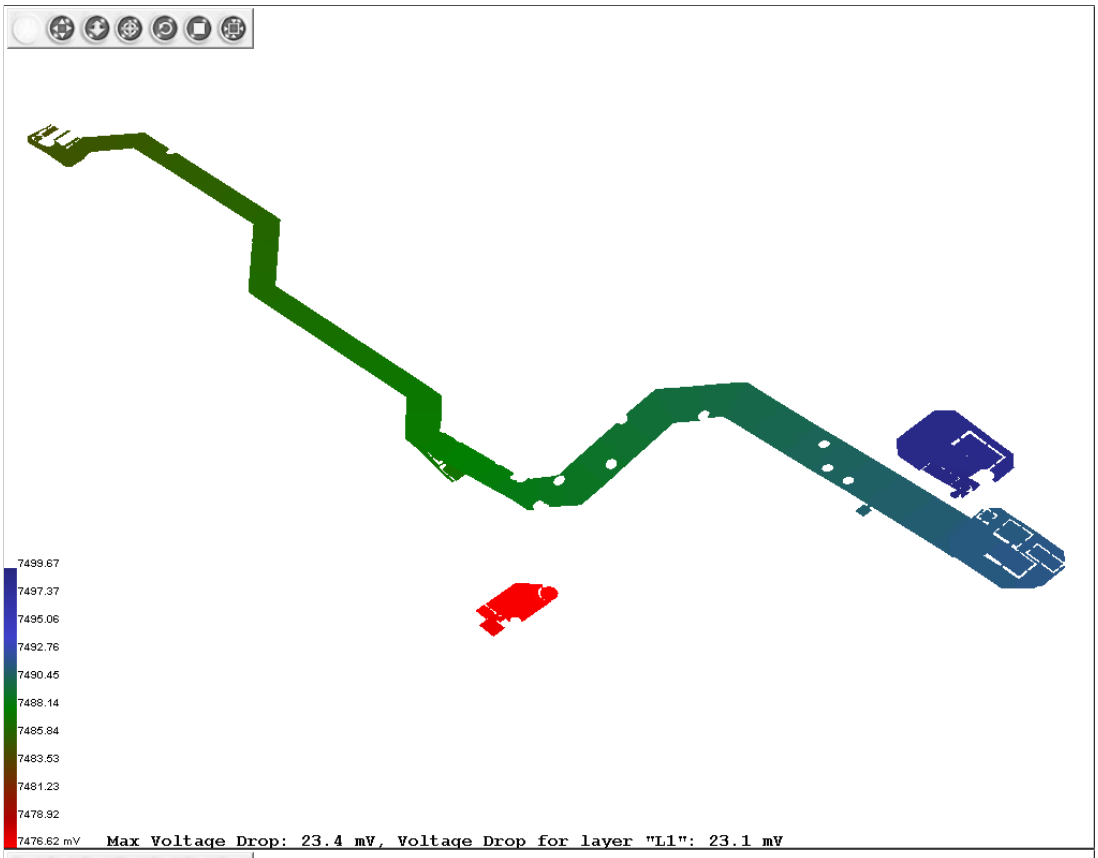
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,034mm	3,5	
3	L1	Copper	0,035mm		
4	Dielectric1	FR4	0,180mm	3,66	
5	P2	Copper	0,035mm		
6	Dielectric 2	FR4	0,710mm	4,2	
7	L3	Copper	0,035mm		
8	Dielectric 3	FR4	0,450mm	4,2	
9	L4	Copper	0,035mm		
10	Bottom Solder	Solder Resist	0,034mm	3,5	
11	Bottom Overlay				

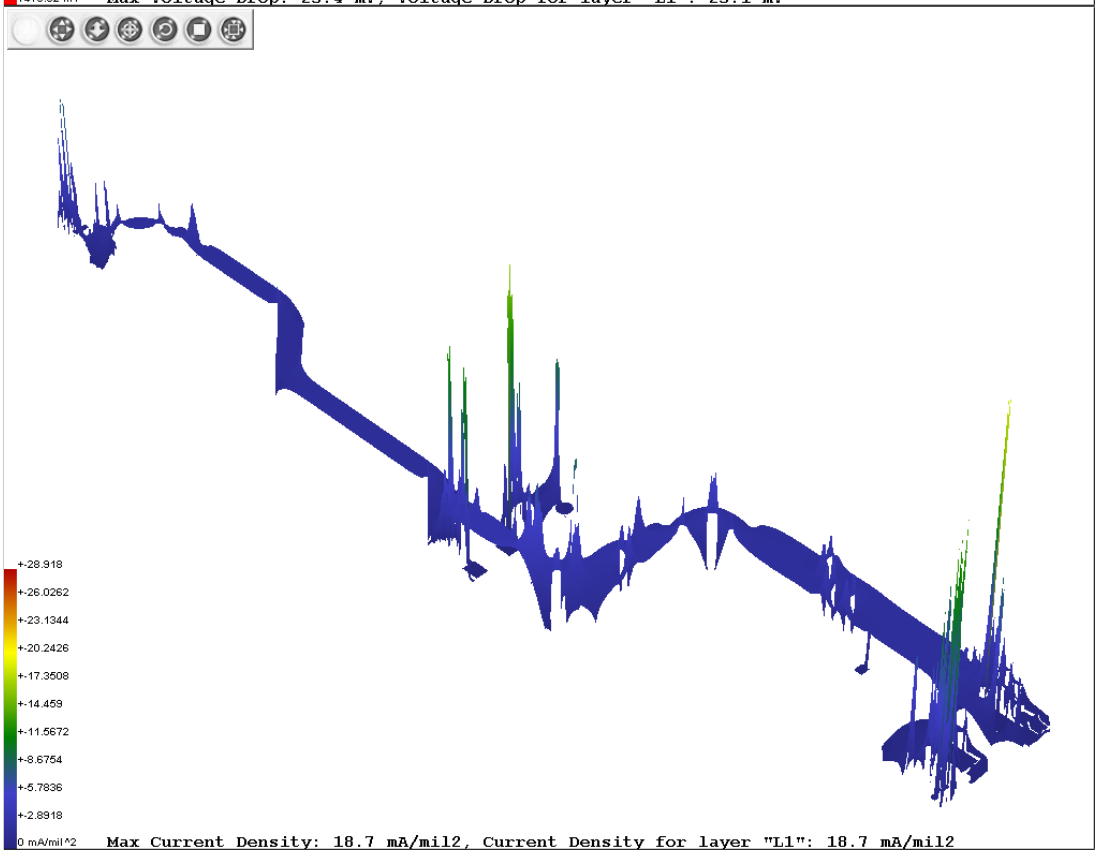
8.4 Appendix D - PowerScope simulation

Voltage drop and current density on P12V0 rail

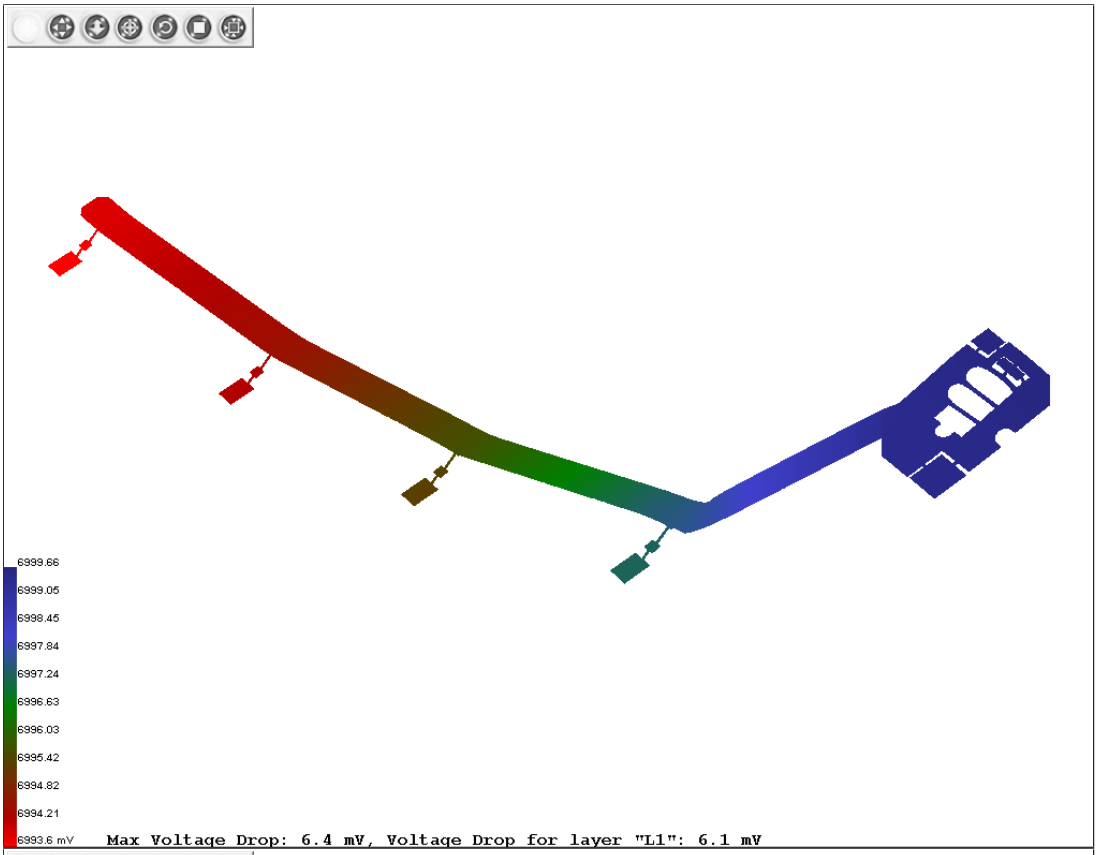


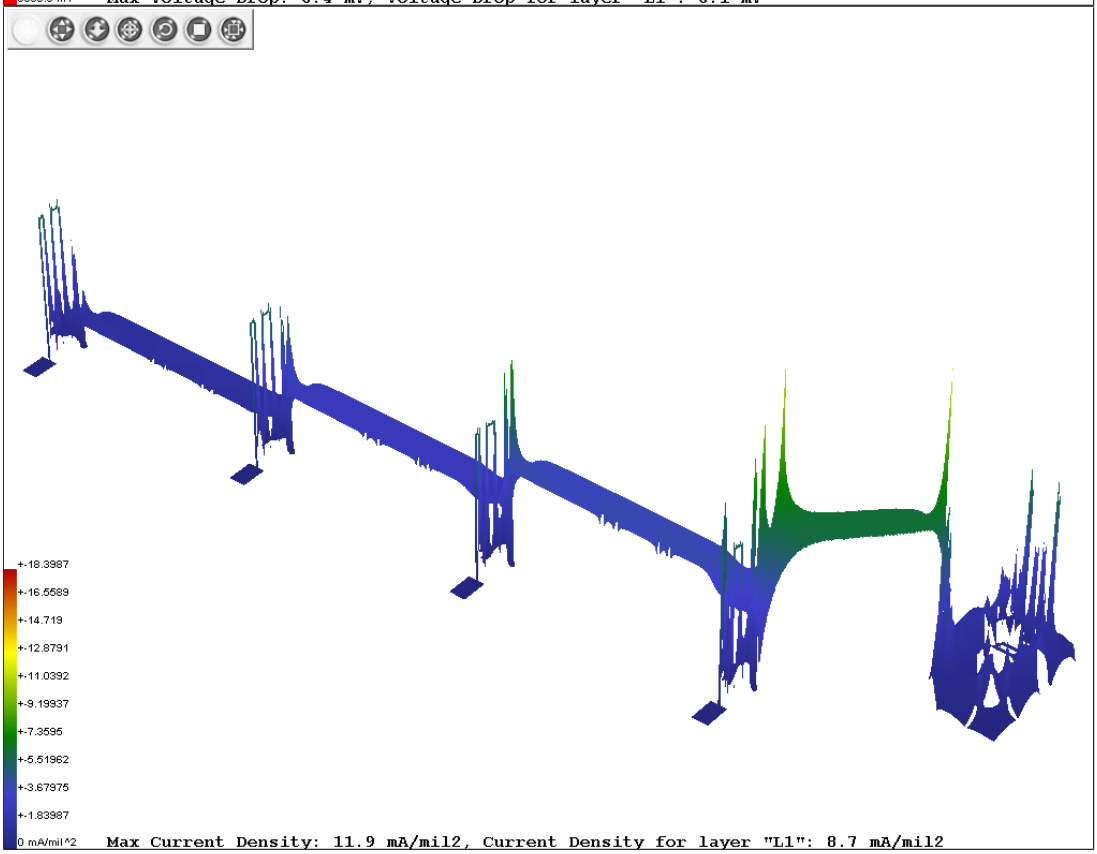
Voltage drop and current density on P7V5 rail



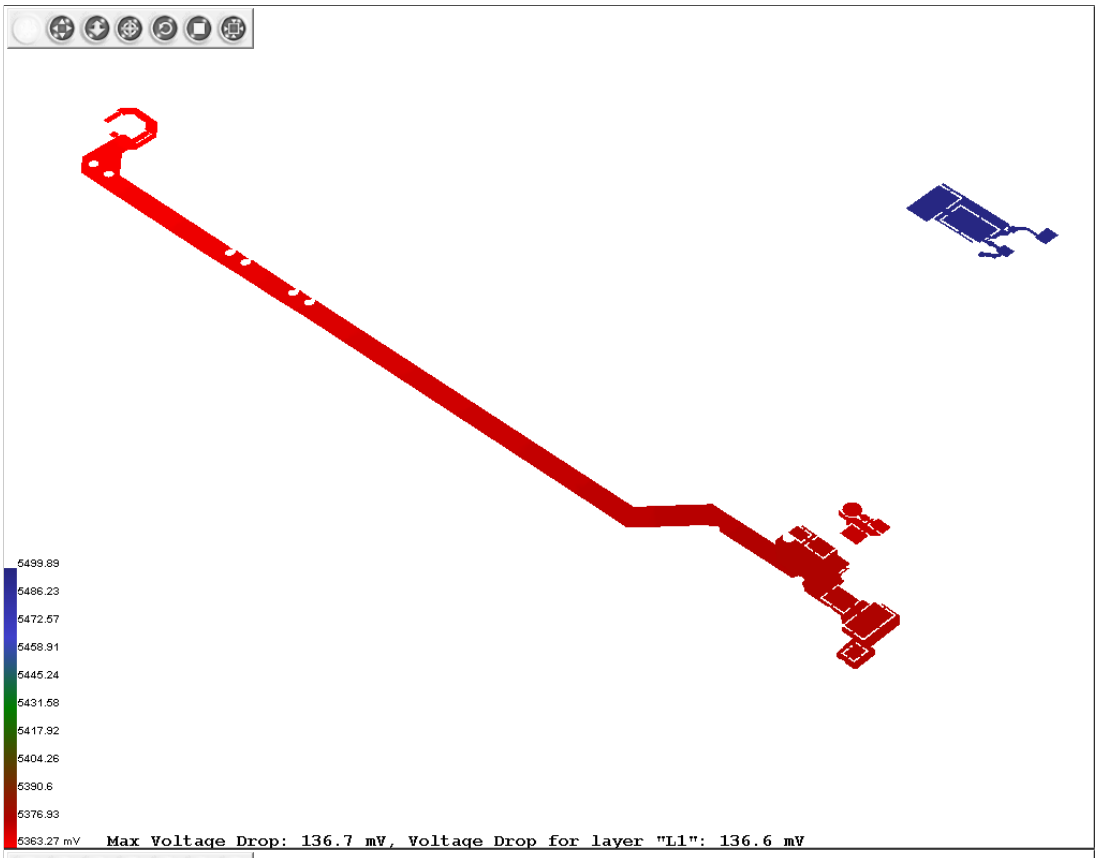


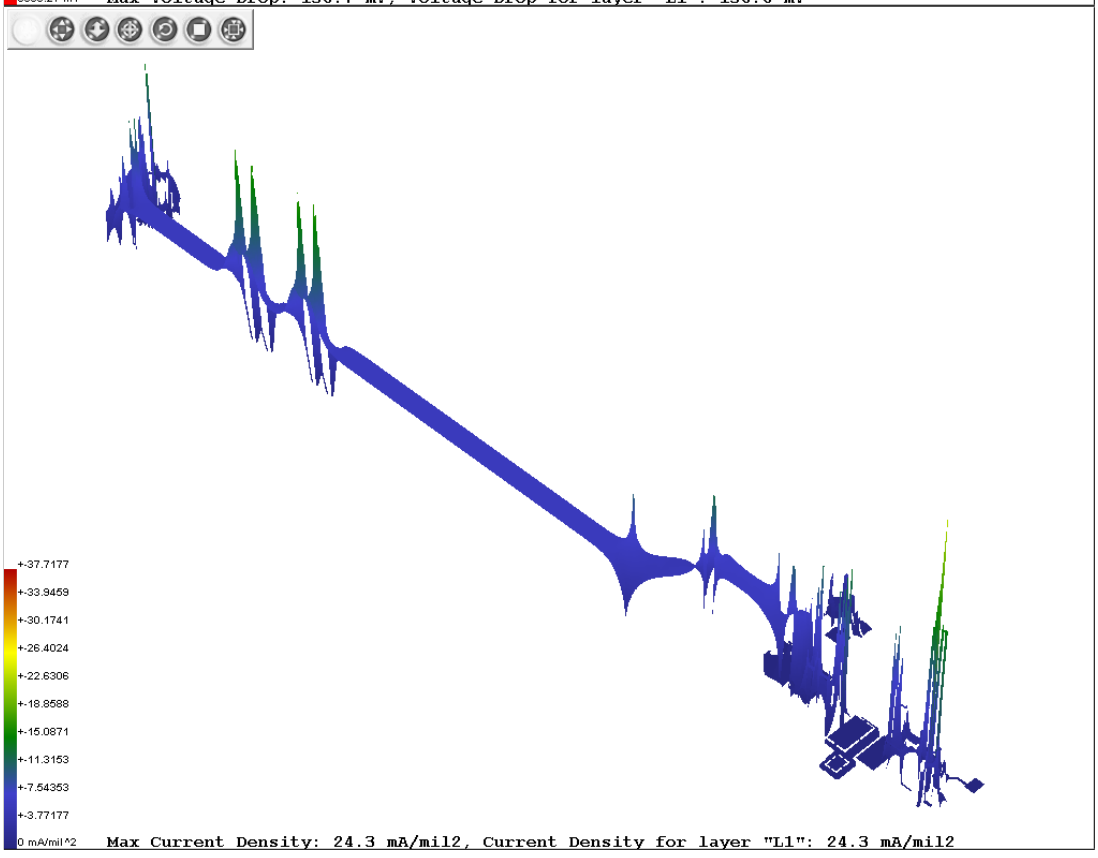
Voltage drop and current density on P7V0A rail



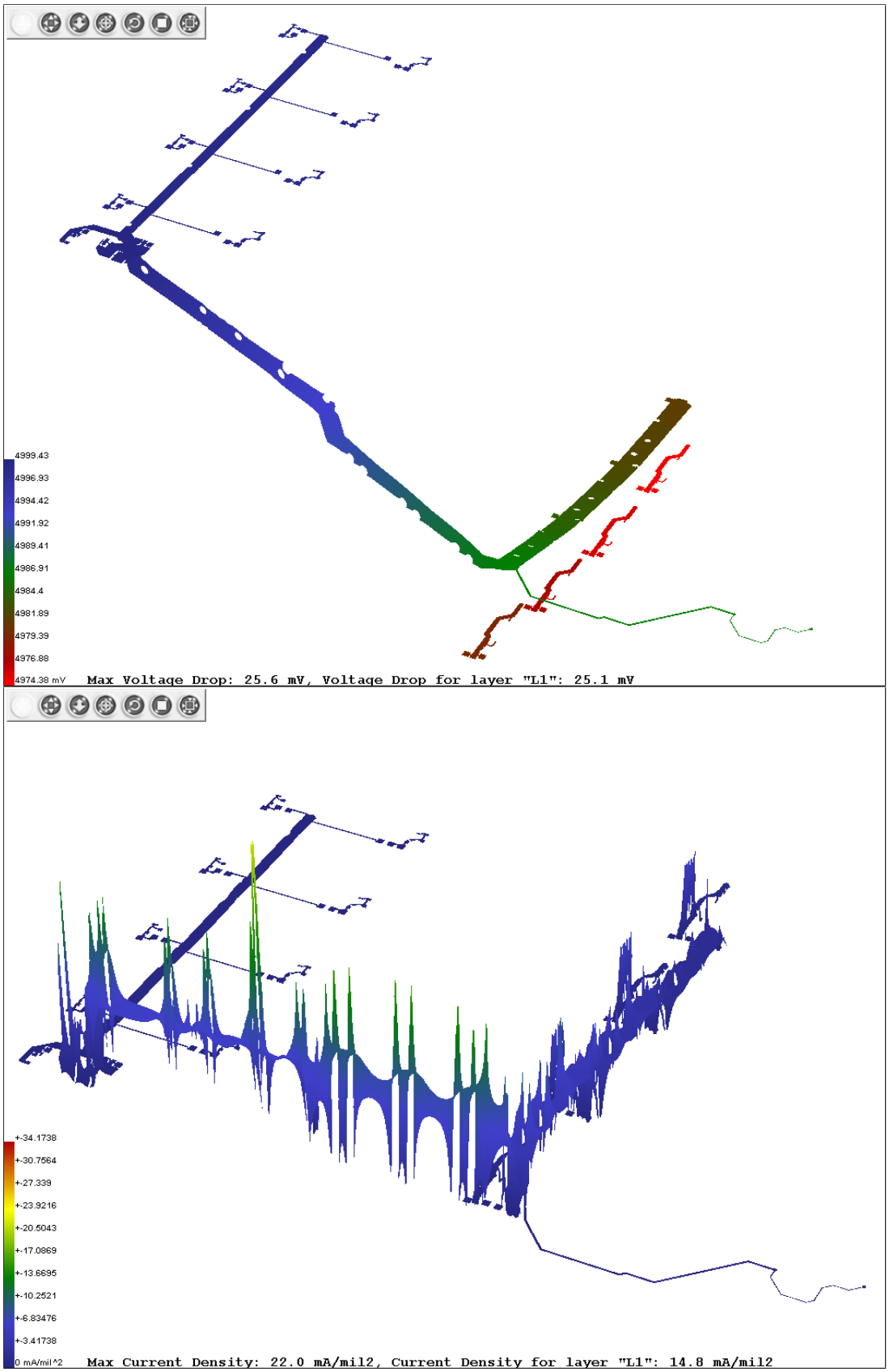


Voltage drop and current density on P5V5A rail

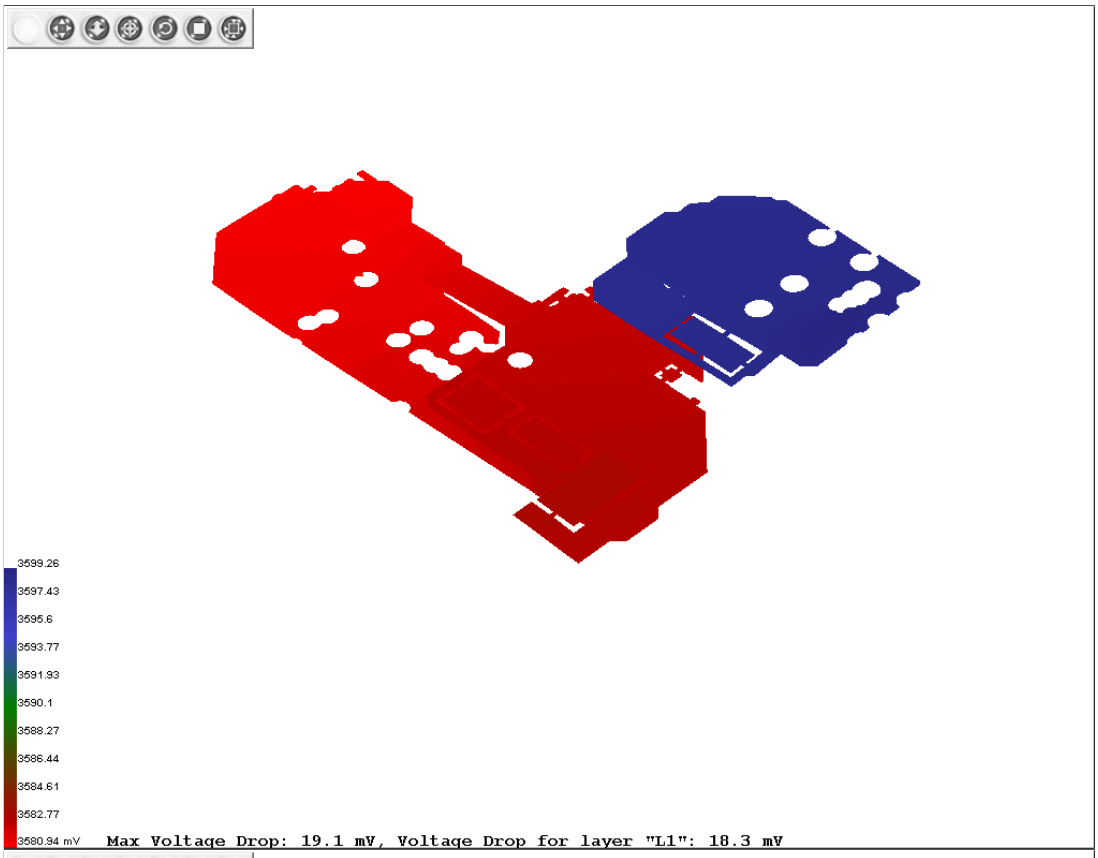


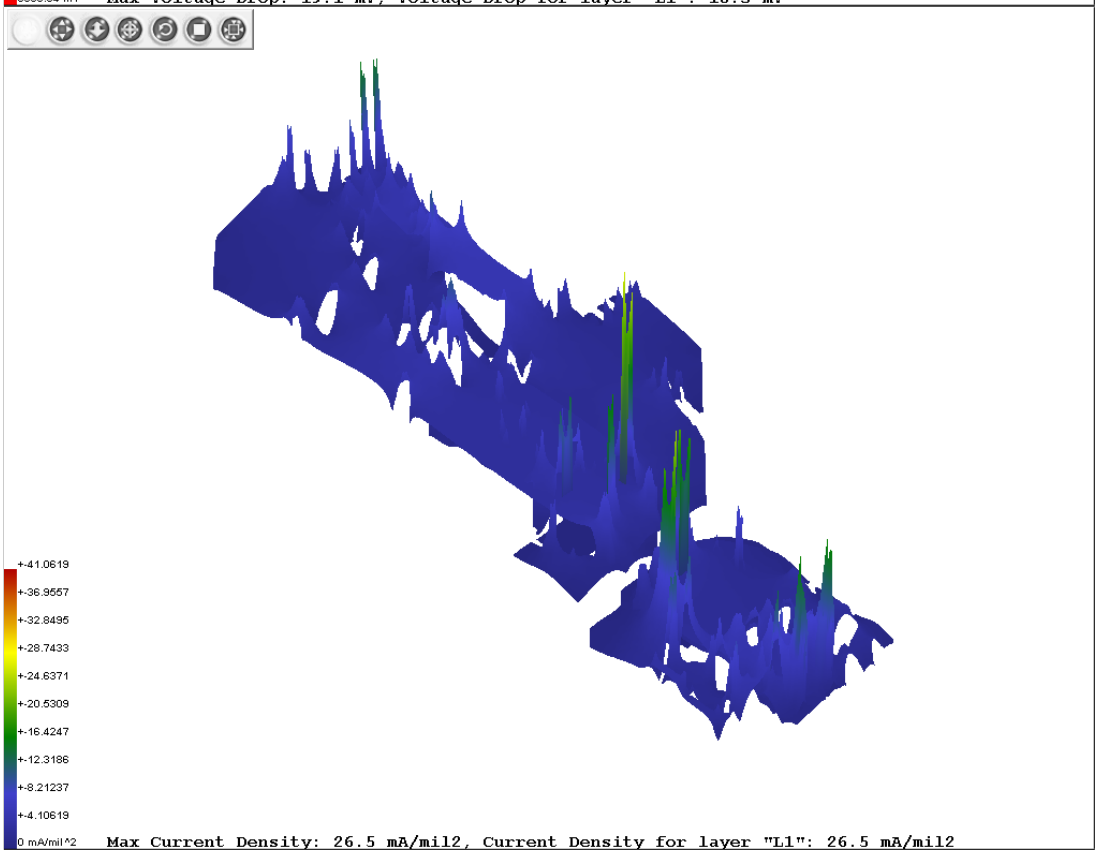


Voltage drop and current density on P5V0A rail

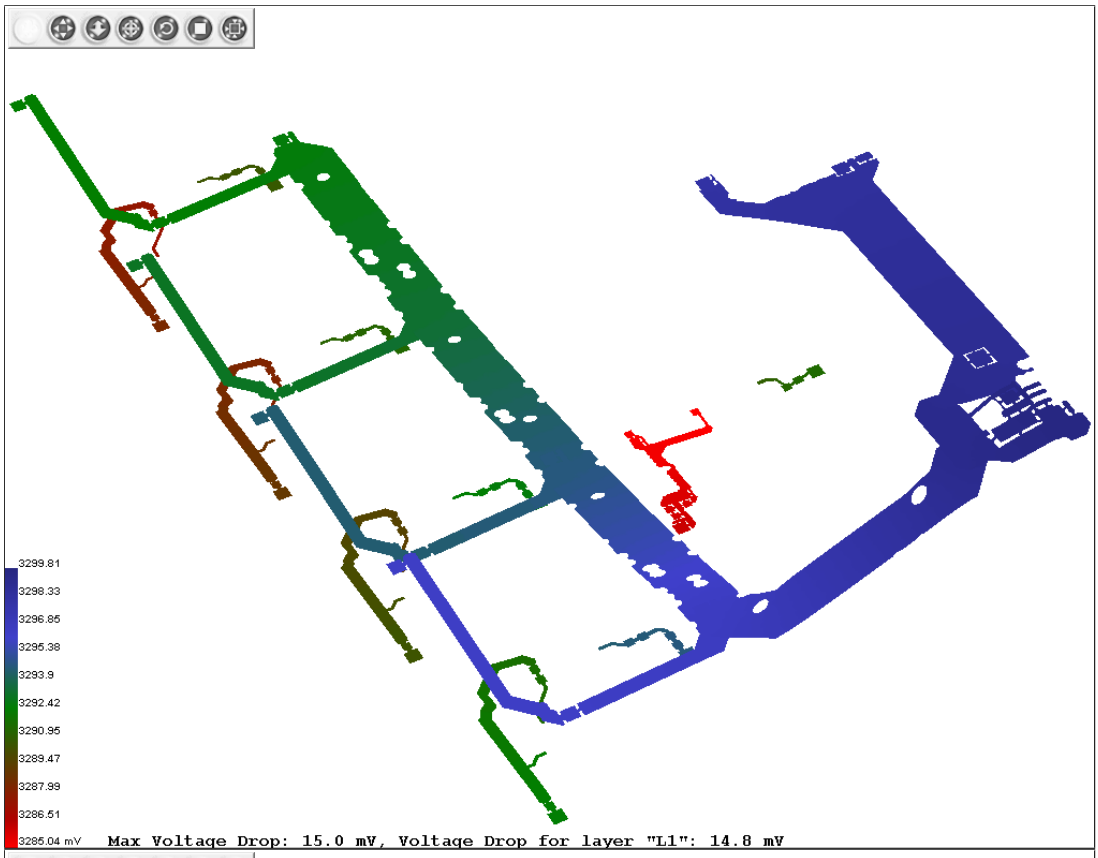


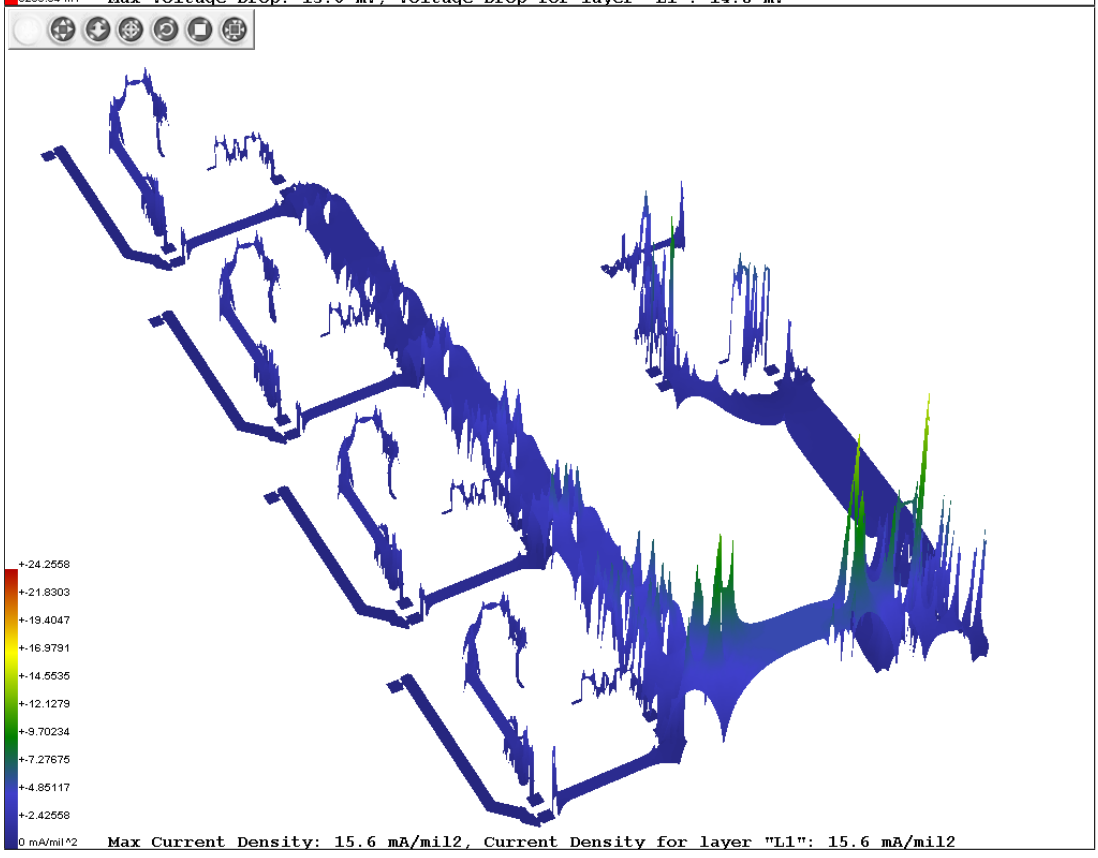
Voltage drop and current density on P3V6 rail



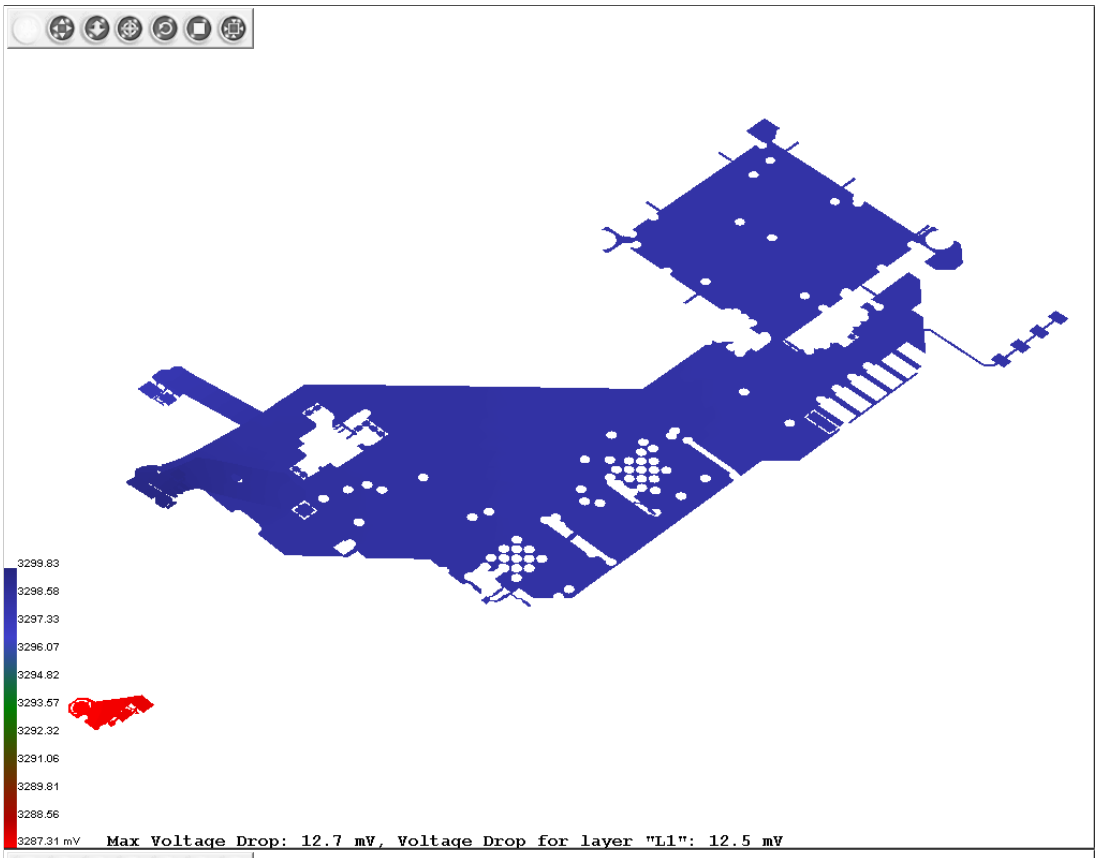


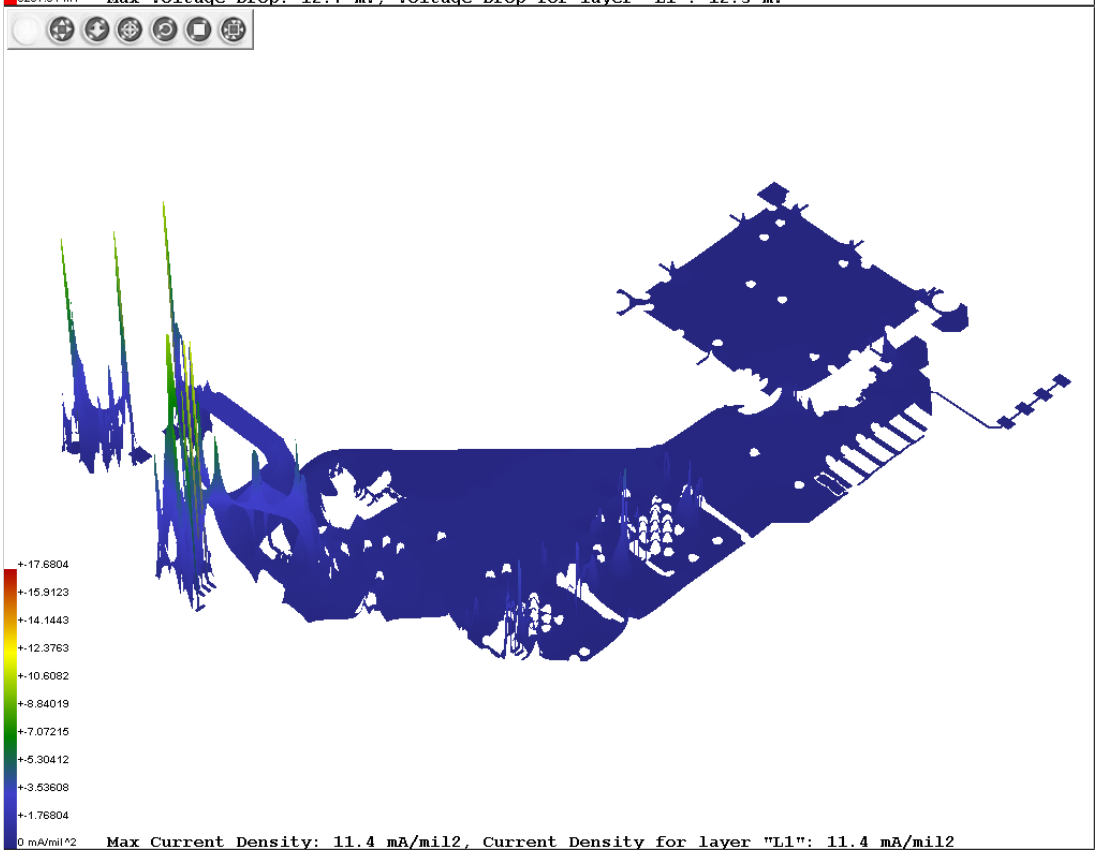
Voltage drop and current density on P3V3A rail





Voltage drop and current density on P3V3 rail





8.5 Appendix E - CPLD code

File: Mirny.v

```
module top(
  output clk_div,
  output clk_in_sel,
  output clk_in_sel_1,
  input [3:0] ifc_mode,
  output [3:0] att_clk,
  output [3:0] att_le,
  output [3:0] att_rst_n,
  output [3:0] att_s_in,
  input [3:0] att_s_out,
  output vco_rf_sw,
  output vco_rf_sw_1,
  output vco_rf_sw_2,
  output vco_rf_sw_3,
  output [1:0] vco_led,
  input vco_muxout,
  output vco_sck,
  output vco_sdi,
  output vco_ce,
  output vco_le,
  output [1:0] vco_led_1,
  input vco_muxout_1,
  output vco_sck_1,
  output vco_sdi_1,
  output vco_ce_1,
  output vco_le_1,
  output [1:0] vco_led_2,
  input vco_muxout_2,
  output vco_sck_2,
  output vco_sdi_2,
  output vco_ce_2,
  output vco_le_2,
  output [1:0] vco_led_3,
  input vco_muxout_3,
  output vco_sck_3,
  output vco_sdi_3,
  output vco_ce_3,
  output vco_le_3,
  inout eem_io,
  output eem_oe,
  inout eem_io_1,
```

```
42    output eem_oe_1,
43    inout eem_io_2,
44    output eem_oe_2,
45    inout eem_io_3,
46    output eem_oe_3,
47    inout eem_io_4,
48    output eem_oe_4,
49    inout eem_io_5,
50    output eem_oe_5,
51    inout eem_io_6,
52    output eem_oe_6,
53    inout eem_io_7,
54    output eem_oe_7,
55    output tp,
56    output tp_1,
57    output tp_2,
58    output tp_3,
59    output tp_4
60 );
61
62 assign clk_div = 1'b0;
63
64 assign clk_in_sel = 1'b0;
65 assign clk_in_sel_1 = 1'b0;
66
67 assign att_clk = 1'b0;
68 assign att_le = 1'b0;
69 assign att_rst_n = 1'b0;
70 assign att_s_in = 1'b0;
71
72 assign vco_rf_sw = 1'b1;
73 assign vco_rf_sw_1 = 1'b1;
74 assign vco_rf_sw_2 = 1'b1;
75 assign vco_rf_sw_3 = 1'b1;
76
77 assign vco_sck  = (ifc_mode[0] == 1) ? eem_io : 1'b0;
78 assign vco_sdi  = (ifc_mode[0] == 1) ? eem_io_1 : 1'b0;
79 assign vco_ce     = 1'b1;
80 assign vco_le     = (ifc_mode[0] == 1) ? eem_io_3 : 1'b0;
81 assign vco_sck_1  = (ifc_mode[1] == 1) ? eem_io : 1'b0;
82 assign vco_sdi_1  = (ifc_mode[1] == 1) ? eem_io_1 : 1'b0;
83 assign vco_ce_1   = 1'b1;
84 assign vco_le_1   = (ifc_mode[1] == 1) ? eem_io_3 : 1'b0;
85 assign vco_sck_2  = (ifc_mode[2] == 1) ? eem_io : 1'b0;
```

```
86  assign vco_sdi_2  = (ifc_mode[2] == 1) ? eem_io_1 : 1'b0;
87  assign vco_ce_2   = 1'b1;
88  assign vco_le_2   = (ifc_mode[2] == 1) ? eem_io_3 : 1'b0;
89  assign vco_sck_3  = (ifc_mode[3] == 1) ? eem_io : 1'b0;
90  assign vco_sdi_3  = (ifc_mode[3] == 1) ? eem_io_1 : 1'b0;
91  assign vco_ce_3   = 1'b1;
92  assign vco_le_3   = (ifc_mode[3] == 1) ? eem_io_3 : 1'b0;
93
94  assign vco_led[0] = vco_muxout;
95  assign vco_led_1[0] = vco_muxout_1;
96  assign vco_led_2[0] = vco_muxout_2;
97  assign vco_led_3[0] = vco_muxout_3;
98
99  assign vco_led[1] = ifc_mode[0];
100 assign vco_led_1[1] = ifc_mode[1];
101 assign vco_led_2[1] = ifc_mode[2];
102 assign vco_led_3[1] = ifc_mode[3];
103
104 assign eem_io_4 = vco_muxout;
105
106 assign eem_oe = 1'b0;
107 assign eem_oe_1 = 1'b0;
108 assign eem_oe_2 = 1'b0;
109 assign eem_oe_3 = 1'b0;
110 assign eem_oe_4 = 1'b1;
111 assign eem_oe_5 = 1'b0;
112 assign eem_oe_6 = 1'b0;
113 assign eem_oe_7 = 1'b0;
114
115 assign tp = eem_io;
116 assign tp_1 = eem_io_1;
117 assign tp_2 = eem_io_2;
118 assign tp_3 = eem_io_3;
119 assign tp_4 = eem_io_4;
120
121 endmodule
```

File: Mirny.ucf

```
NET "clk_div" LOC=P53; # clk:0.div
NET "clk_in_sel" LOC=P54; # clk:0.in_sel
NET "clk_in_sel_1" LOC=P56; # clk:0.in_sel_1
NET "ifc_mode(0)" LOC=P102 | PULLUP; # ifc_mode:0
NET "ifc_mode(1)" LOC=P103 | PULLUP; # ifc_mode:0
NET "ifc_mode(2)" LOC=P104 | PULLUP; # ifc_mode:0
NET "ifc_mode(3)" LOC=P105 | PULLUP; # ifc_mode:0
NET "att_clk(0)" LOC=P131; # att:0.clk
NET "att_le(0)" LOC=P132; # att:0.le
NET "att_rst_n(0)" LOC=P130; # att:0.rst_n
NET "att_s_in(0)" LOC=P133; # att:0.s_in
NET "att_s_out(0)" LOC=P129; # att:0.s_out
NET "att_clk(1)" LOC=P3; # att:1.clk
NET "att_le(1)" LOC=P4; # att:1.le
NET "att_rst_n(1)" LOC=P2; # att:1.rst_n
NET "att_s_in(1)" LOC=P5; # att:1.s_in
NET "att_s_out(1)" LOC=P134; # att:1.s_out
NET "att_clk(2)" LOC=P9; # att:2.clk
NET "att_le(2)" LOC=P10; # att:2.le
NET "att_rst_n(2)" LOC=P7; # att:2.rst_n
NET "att_s_in(2)" LOC=P11; # att:2.s_in
NET "att_s_out(2)" LOC=P6; # att:2.s_out
NET "att_clk(3)" LOC=P14; # att:3.clk
NET "att_le(3)" LOC=P15; # att:3.le
NET "att_rst_n(3)" LOC=P13; # att:3.rst_n
NET "att_s_in(3)" LOC=P16; # att:3.s_in
NET "att_s_out(3)" LOC=P12; # att:3.s_out
NET "vco_rf_sw" LOC=P136; # vco:0.rf_sw
NET "vco_rf_sw_1" LOC=P138; # vco:1.rf_sw
NET "vco_rf_sw_2" LOC=P140; # vco:2.rf_sw
NET "vco_rf_sw_3" LOC=P143; # vco:3.rf_sw
NET "vco_led(0)" LOC=P110; # vco:0.led
NET "vco_led(1)" LOC=P111; # vco:0.led
NET "vco_led_1(0)" LOC=P112; # vco:1.led
NET "vco_led_1(1)" LOC=P113; # vco:1.led
NET "vco_led_2(0)" LOC=P115; # vco:2.led
NET "vco_led_2(1)" LOC=P116; # vco:2.led
NET "vco_led_3(0)" LOC=P117; # vco:3.led
NET "vco_led_3(1)" LOC=P118; # vco:3.led
NET "vco_muxout" LOC=P24 | PULLUP; # vco:0.muxout
NET "vco_sck" LOC=P23; # vco:0.sck
NET "vco_sdi" LOC=P22; # vco:0.sdi
NET "vco_ce" LOC=P19; # vco:0.ce
```

```
NET "vco_le" LOC=P21; # vco:0.le
NET "vco_muxout_1" LOC=P25 | PULLUP; # vco:1.muxout
NET "vco_sck_1" LOC=P26; # vco1.sck
NET "vco_sdi_1" LOC=P32; # vco:1.sdi
NET "vco_ce_1" LOC=P28; # vco:1.ce
NET "vco_le_1" LOC=P30; # vco:1.le
NET "vco_muxout_2" LOC=P35 | PULLUP; # vco:2.muxout
NET "vco_sck_2" LOC=P39; # vco:2.sck
NET "vco_sdi_2" LOC=P43; # vco:2.sdi
NET "vco_ce_2" LOC=P40; # vco:2.ce
NET "vco_le_2" LOC=P41; # vco:2.le
NET "vco_muxout_3" LOC=P45 | PULLUP; # vco:3.muxout
NET "vco_sck_3" LOC=P49; # vco:3.sck
NET "vco_sdi_3" LOC=P52; # vco:3.sdi
NET "vco_ce_3" LOC=P50; # vco:3.ce
NET "vco_le_3" LOC=P51; # vco:3.le
NET "eem_io" LOC=P38; # eem:0.io
NET "eem_oe" LOC=P81; # eem:0.oe
NET "eem_io_1" LOC=P70; # eem:1.io
NET "eem_oe_1" LOC=P82; # eem:1.oe
NET "eem_io_2" LOC=P71; # eem:2.io
NET "eem_oe_2" LOC=P83; # eem:2.oe
NET "eem_io_3" LOC=P74; # eem:3.io
NET "eem_oe_3" LOC=P85; # eem:3.oe
NET "eem_io_4" LOC=P76; # eem:4.io
NET "eem_oe_4" LOC=P86; # eem:4.oe
NET "eem_io_5" LOC=P77; # eem:5.io
NET "eem_oe_5" LOC=P87; # eem:5.oe
NET "eem_io_6" LOC=P78; # eem:6.io
NET "eem_oe_6" LOC=P88; # eem:6.oe
NET "eem_io_7" LOC=P79; # eem:7.io
NET "eem_oe_7" LOC=P91; # eem:7.oe
NET "tp" LOC=P128; # tp:0
NET "tp_1" LOC=P126; # tp:1
NET "tp_2" LOC=P125; # tp:2
NET "tp_3" LOC=P124; # tp:3
NET "tp_4" LOC=P121; # tp:4
#NET "MMCX_OSCn_SEL" LOC=P136; # tp:3
#NET "OSC_ENn" LOC=P134; # tp:4

NET "eem_io" TNM_NET = "PRDeem_io";
TIMESPEC "TSeem_io" = PERIOD "PRDeem_io" 8.0 ns HIGH 50%;
```