

5632 DAC Fastino

Features

- 32-channel fast DAC
- 16-bit resolution
- 2.55 MSPS per channel
- Output voltage $\pm 10V$
- Gateware CIC interpolation
- HD68 connector
- Can be broken out to BNC/SMA/MCX

Applications

- Controlling setpoints of PID controllers for laser power stabilization
- Low-frequency arbitrary waveform generation
- Driving DC electrodes in ion traps

General Description

The 5632 DAC Fastino is a 4hp EEM module, part of the ARTIQ/Sinara family. It adds digital-analog conversion capabilities to carrier cards such as 1124 Kasli and 1125 Kasli-SoC. It is closely related to the slower 5432 DAC Zotino and the two cards share a compatible output interface.

It provides four groups of eight analog channels each, exposed by one HD68 connector. Each channel supports output voltage from -10 V to 10 V. All channels can be updated simultaneously. Channels can broken out to BNC, SMA or MCX by adding external 5518 BNC-IDC, 5528 SMA-IDC or 5538 MCX-IDC cards.



Figure 1: Fastino card



Figure 2: Fastino front panel

Source

5632 DAC Fastino, like all the Sinara hardware family, is open-source hardware, and design files (schematics, PCB layouts, BOMs) can be found in detail at the repository https://github.com/sinara-hw/Fastino.

Electrical Specifications

These specifications are based on the datasheet of the DAC IC (AD5542ABCPZ¹), and various information from the Sinara wiki².

Parameter	Min.	Тур.	Max.	Unit	Conditions
Output voltage	-10		10	V	
Resolution ¹		16		bits	
Settling time ¹		1		μs	
Temperature coefficient ²			7	ppm	

Table 1: Output Specifications

The following table records cross-talk and transient behavior by Fastino, collected in various Sinara issues, see spur analysis³, cross-talk⁴, and noise summary⁵. DAC output during output noise measurement was 6.875 V, updating continuously, channel 27 used for recording.

Parameter	Min.	Typ.	Max.	Unit	Conditions / Comments
DC cross-talk			-65	dBmV	
Broadband noise (??)					
@ 100 kHz		14		nV/rtHz	
@ 1 MHz		56		nV/rtHz	
Output noise					
@ 500 kHz		60	80	nV/rtHz	
@ 2 MHz			12	nV/rtHz	
@ 10 MHz			4	nV/rtHz	
Spur-free range	0.1		5	MHz	Correctly configured ³
Digital update spurs		560		nVrm	@ 2.55MHz

Table 2: Electrical Characteristics

LEDs

5632 DAC Fastino provides eight user LEDs in the front panel. These are directly accessible in the ARTIQ RTIO. Four additional LEDs indicate, respectively, power good (PG), ??? (FD), overtemperature (OT), and gateware or initialization error (ERR).

¹https://www.analog.com/media/en/technical-documentation/data-sheets/AD5512A_5542A.pdf

²https://github.com/sinara-hw/Fastino/wiki

 $^{^3}$ https://github.com/sinara-hw/Fastino/issues/56

⁴https://github.com/sinara-hw/Fastino/issues/85

⁵https://github.com/sinara-hw/Fastino/issues/51

ARTIQ System Description Entry

ARTIQ/Sinara firmware/gateware is generated according to a JSON system description file, allowing gateware to be specific to and optimized for a certain system configuration.

5632 DAC Fastino should be entered in the peripherals list of the corresponding core device in the following format:

Replace 0 with the EEM port used on the core device. Any port may be used on the core device side. Despite providing two EEM ports, Fastino only requires one of two under ARTIQ control. This should always be EEM0. If connected, EEM1 will be ignored.

The $log2_width$ field accepts a number from 0 to 5 inclusive and represents (in powers of two) the number of DAC channels packed into a single RTIO write (1 to 32). This allows and defines the use of $set_group()$ functions rather than $set_dac()$ as in examples given below.

Example ARTIQ Code

The sections below demonstrate simple usage scenarios of extensions on the ARTIQ control system. These extensions make use of the resources of the 5632 DAC Fastino. They do not exhaustively demonstrate all the features of the ARTIQ system.

The full documentation for ARTIQ software and gateware, including guides for their use, is available at https://m-labs.hk/artiq/manual/. Please consult the manual for details and reference material of the functions and structures used here.

Setting output voltage

The following example initializes the Fastino card, then emits 1.0 V, 2.0 V, 3.0 V and 4.0 V at channels 0, 1, 2, and 3 respectively. Voltage of all 4 channels is updated simultaneously with the use of $set_dac()$.

```
def prepare(self):
    self.channels = [0, 1, 2, 3]
    self.voltages = [1.0, 2.0, 3.0, 4.0]

@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.dac.init()

    delay(1*ms)
    self.dac.set_dac(self.voltages, self.channels)
```

Triangular wave

The following example generates a triangular waveform at 10 Hz, 16 V peak-to-peak. Timing accuracy of the RTIO system can be demonstrated by the precision of the frequency.

Import scipy.signal and numpy modules to run this example.

```
def prepare(self):
    self.period = 0.1*s
    self.sample = 128
    t = numpy.linspace(0, 1, self.sample)
    self.voltages = 8*signal.sawtooth(2*numpy.pi*t, 0.5)
    self.interval = self.period/self.sample
@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.dac.init()
    delay(1*ms)
    counter = 0
    while True:
        self.dac.set_dac([self.voltages[counter]], [0])
        counter = (counter + 1) % self.sample
        delay(self.interval)
```

CIC interpolators

Fastino gateware features dynamically configurable CIC (cubic B-spline) interpolators, defined individually by channel, with interpolation rates from 1 (2.55 MSPS) to 65536 (39 SPS). For more details, see manual documentation on ARTIQ driver functions stage_cic and apply_cic.

Ordering Information

To order, please visit https://m-labs.hk and choose 5632 DAC Fastino in the ARTIQ/Sinara hardware selection tool. Cards can be ordered as part of a fully-featured ARTIQ/Sinara crate or standalone through the 'Spare cards' option. Otherwise, orders can also be made by writing directly to mailto:sales@m-labs.hk.

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