4410/4412 DDS Urukul

Features

- 4-channel 1GS/s DDS
- Output frequency from <1 to >400 MHz
- Sub-Hz frequency resolution
- Controlled phase steps
- Accurate output amplitude control

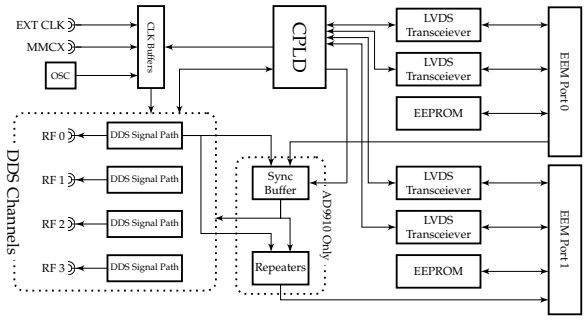


Figure 1: Simplified Block Diagram

Applications

- Dynamic low-noise RF source
- Driving RF electrodes in ion traps
- Driving acousto-optic modulators
- Form a laser intensity servo with 5108 Sampler

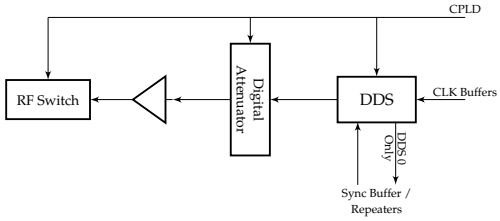


Figure 2: Simplified DDS Signal Path

General Description

The 4410/4412 DDS Urukul card is a 4hp EEM module, part of the ARTIQ/Sinara family. It adds frequency generation capabilities to carrier cards such as 1124 Kasli and 1125 Kasli-SoC.

It provides 4 channels of DDS (direct digital synthesis) at 1GS/s. Output frequencies from <1 to >400 MHz are supported. The nominal maximum output power of each channel is 10dBm. Each channel can be attenuated from 0 to -31.5 dB by a digital attenuator. RF switches (1ns temporal resolution) on each channel provide 70 dB isolation.

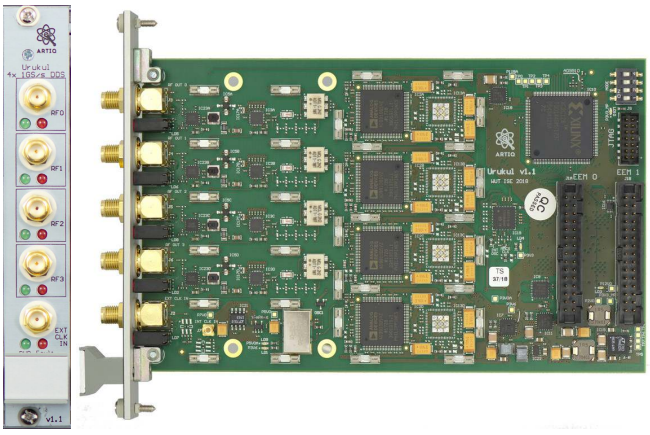


Figure 3: Urukul card and front panel

4410 DDS Urukul features AD9910 chips, while 4412 DDS Urukul features AD9912 chips. AD9912 is capable of higher frequency precision (8 µHz) than the AD9910 (0.25 Hz). The ARTIQ SU-Servo configuration is only available for AD9910.

Source

4410/4412 DDS Urukul, like all the Sinara hardware family, is open-source hardware, and design files (schematics, PCB layouts, BOMs) can be found in detail at the repository https://github.com/sinara-hw/Urukul/.

Electrical Specifications

Specifications of parameters are based on the datasheets of the DDS IC (AD9910[1], AD9912[2]), clock buffer IC (Si53312[3]), digital attenuator IC (HMC542BLP4E[4]), Sinara project information[5] and corresponding test results[6].

Table 1: Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Conditions
Clock input					
Input frequency[1,2]	10		1000	MHz	PLL disabled
	3.2		60	MHz	AD9910, PLL enabled, no clock division
	12.8		240	MHz	AD9910, PLL enabled, 4x clock division
	11		200	MHz	AD9912, PLL enabled, no clock division
	44		800	MHz	AD9912, PLL enabled, 4x clock division
Nominal input power[3]		10		dBm	

Table 2: RF Output Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
Low frequency power[6]			-20	dBm	100 kHz output
			10	dBm	1 MHz output
Frequency[5]	1		400	MHz	
Digital attenuation[4]	-31.5		0	dB	
Resolution					
Frequency[1,5]		0.25		Hz	AD9910
		8		μHz	AD9912
Phase offset[1,2]		16/14		bits	AD9910/AD9912 respectively
Digital amplitude[1]		14		bits	AD9910
DAC full scale current[1,2]		8/10		bits	AD9910/AD9912 respectively
Temporal (I/O Update)[5]		4		ns	
Digital attenuation[4]		0.5		dB	

[1] https://www.analog.com/media/en/technical-documentation/data-sheets/AD9910.pdf
[2] https://www.analog.com/media/en/technical-documentation/data-sheets/AD9912.pdf
[3] https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/Si53312.pdf
[4] https://www.analog.com/media/en/technical-documentation/data-sheets/hmc542b.pdf
[5] https://github.com/sinara-hw/Urukul/wiki#details-specification-and-typical-performance-data
[6] https://github.com/sinara-hw/sinara/issues/354#issuecomment-352859041

The tabulated performance characteristics are produced using the following setup unless otherwise noted:

- 100 MHz input clock into SMA, 10 dBm
- Input clock divided by 4
- PLL with x40 multiplier
- Output frequency at 80 MHz or 81 MHz

Table 3: Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital attenuator glitch duration[6]	t_s		100		ns	
RF switch[6]						
Rise to 90%	t_{on}		100		ns	
Isolation			70		dB	
Turn-on chirp	γ			0.1	deg/s	Excluding the first μs
Crosstalk[6]			-84		dB	Victim RF switch opened
			-110		dB	Victim RF switch closed
Cross-channel-intermodulation[6]			-90		dB	
Phase noise[6]	$\mathcal{L}(f)$		-85		dBc/Hz	0.1 Hz
			-95		dBc/Hz	1 Hz
			-107		dBc/Hz	10 Hz
			-116		dBc/Hz	100 Hz
			-126		dBc/Hz	1 kHz
			-133		dBc/Hz	10 kHz
			-135		dBc/Hz	100 kHz
			-128		dBc/Hz	1 MHz
			-149		dBc/Hz	10 MHz
Second-order harmonics[6]			-40		dB	6 dBm output
			-34		dB	10.5 dBm output
Third-order harmonics[6]			-54		dB	6 dBm output
			-28		dB	10.5 dBm output
Power consumption (AD9910)[5]	P		7		W	4x 400 MHz, 10.5 dBm, 52°C
Power consumption (AD9912)[5]	P		6.5		W	4x 400 MHz, 10.5 dBm, 52°C

Harmonic content of the DDS signals from 4410 DDS Urukul is tabulated below[7]. An external 125 MHz clock signal was supplied.

Table 4: Harmonic content with 0.0 dB digital attenuation

Frequency (MHz)	Output power (dBm) of the nth-order harmonic								
	1st	2nd	3rd	4th	5th	6th	7th	8th	9th
0.1	-21.14	-59.03	-54.93	-93.07	-73.38	-94.07	-84.78	-91.77	-96.61
0.5	4.51	-15.45	-11.61	-25.02	-24.35	-51.70	-35.14	-34.46	-37.85
1	7.67	-16.80	-12.32	-18.27	-29.25	-30.87	-34.51	-39.28	-39.84
10	10.67	-12.69	-13.94	-26.12	-27.76	-36.11	-55.32	-43.85	-42.65
20	10.86	-24.90	-13.65	-22.87	-28.67	-47.68	-35.85	-35.45	-38.48
50	10.74	-14.18	-15.01	-27.57	-29.01	-38.05	-51.52	-44.53	-42.71
100	9.70	-33.59	-16.72	-34.36	-26.81	-40.14	-41.07	-43.88	-56.89
200	8.97	-22.22	-16.23	-24.89	-30.49	-37.97	-37.79	-38.80	-40.14
300	8.27	-19.17	-19.51	-29.80	-34.75	-38.90	-51.92	-53.38	-57.95
400	7.68	-17.82	-21.60	-33.04	-37.80	-50.37	-57.45	-59.80	-64.68
500	-1.80	-41.57	-51.71	-72.36	-89.35	-91.63	-93.15	-84.54	-107.57

Table 5: Harmonic content with 10.0 dB digital attenuation

Frequency (MHz)	Output power (dBm) of the nth-order harmonic								
	1st	2nd	3rd	4th	5th	6th	7th	8th	9th
0.1	-27.06	-81.35	-62.09	-97.37	-84.11	-103.78	-91.37	-100.48	-104.22
0.5	-3.2	-37.82	-52.21	-66.76	-77.86	-85.92	-86.37	-97.59	-120.76
1	-0.43	-34.47	-47.80	-75.28	-86.45	-101.91	-93.22	-96.14	-106.71
10	1.95	-31.04	-28.23	-51.76	-57.29	-76.26	-78.15	-83.85	-80.20
20	2.10	-33.05	-28.30	-54.50	-52.31	-72.39	-70.96	-82.98	-82.58
50	1.89	-33.24	-28.50	-52.67	-48.35	-74.77	-77.26	-79.33	-73.58
100	0.80	-38.51	-63.22	-61.73	-71.97	-97.45	-97.67	-107.40	-93.03
200	0.05	-38.25	-42.16	-63.01	-84.55	-82.66	-108.85	-116.62	-99.45
300	-0.51	-35.91	-48.83	-82.43	-100.53	-111.79	-118.62	-120.05	-97.72
400	-1.20	-38.37	-49.77	-89.45	-74.66	-108.12	-116.75	-114.08	-102.29
500	-11.20	-61.47	-77.59	-74.73	-100.23	-93.12	-99.83	-86.71	-112.63

[7] https://github.com/sinara-hw/Urukul/issues/29

Table 6: Harmonic content with 20.0 dB digital attenuation

Frequency (MHz)	Output power (dBm) of the n^{th}-order harmonic								
	1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}	6^{th}	7^{th}	8^{th}	9^{th}
0.1	-31.06	-82.29	-68.34	-109.04	-92.48	-111.23	-99.94	-109.85	-112.36
0.5	-11.99	-56.69	-71.73	-95.76	-101.86	-114.37	-102.81	-106.94	-116.72
1	-9.94	-54.54	-56.49	-89.12	-105.94	-110.93	-102.79	-107.01	-117.29
10	-7.89	-50.19	-57.35	-91.36	-97.88	-107.95	-103.53	-96.04	-108.26
20	-7.79	-52.72	-58.03	-90.75	-99.82	-102.07	-101.55	-104.73	-103.31
50	-7.96	-52.36	-59.26	-84.44	-87.55	-86.88	-97.76	-92.61	-83.19
100	-9.04	-57.40	-61.76	-78.50	-91.80	-117.64	-107.40	-112.64	-102.07
200	-9.73	-57.39	-72.31	-72.66	-93.26	-95.95	-125.22	-122.35	-130.24
300	-10.27	-58.65	-74.60	-109.24	-107.74	-115.75	-125.36	-124.54	-98.86
400	-10.94	-59.62	-79.36	-98.48	-74.72	-111.95	-119.18	-114.63	-104.34
500	-21.00	-78.52	-99.07	-74.91	-99.55	-92.91	-103.02	-87.33	-114.87

Table 7: Harmonic content with 31.5 dB digital attenuation

Frequency (MHz)	Output power (dBm) of the n^{th}-order harmonic								
	1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}	6^{th}	7^{th}	8^{th}	9^{th}
0.1	-37.89	-85.04	-77.41	-122.04	-114.29	-115.58	-110.65	-120.06	-123.70
0.5	-22.38	-71.24	-89.84	-107.81	-108.76	-127.83	-114.12	-118.34	-127.07
1	-21.01	-72.10	-90.08	-111.97	-111.30	-127.43	-114.38	-118.07	-128.06
10	-19.22	-72.13	-90.74	-110.14	-105.28	-114.04	-113.51	-94.85	-116.15
20	-19.28	-75.95	-94.72	-91.71	-107.55	-112.85	-112.24	-116.33	-114.02
50	-19.27	-74.93	-92.21	-95.77	-101.06	-97.92	-108.30	-103.60	-93.96
100	-20.27	-79.05	-87.48	-89.73	-104.00	-117.98	-112.12	-110.51	-105.80
200	-21.19	-78.33	-106.81	-82.70	-92.31	-109.93	-133.86	-120.94	-102.95
300	-21.58	-80.96	-112.44	-110.40	-108.11	-115.68	-122.51	-125.25	-99.63
400	-22.44	-82.73	-105.55	-98.03	-74.84	-113.93	-119.41	-114.93	-104.55
500	-31.73	-93.37	-99.74	-75.03	-99.27	-92.84	-104.14	-87.46	-116.22

The RMS voltage of a 4410 DDS Urukul channel at different amplitude scale factors is measured below. The DDS channel is directly connected to an oscilloscope with a 50Ω termination. The reported values are obtained from the oscilloscope.

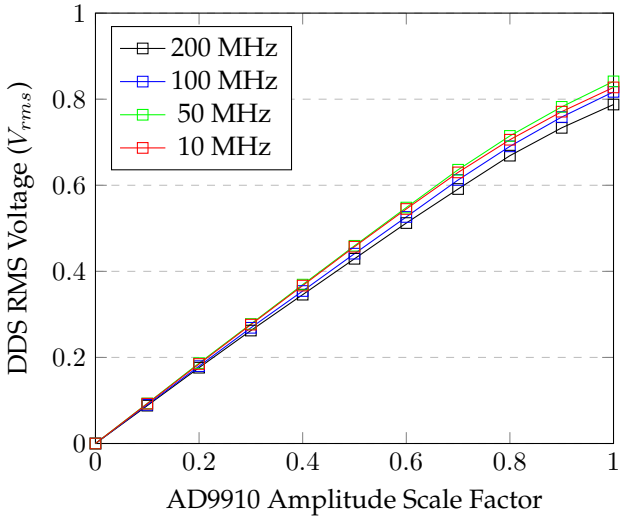


Figure 4: RMS voltage, 0dB attenuation

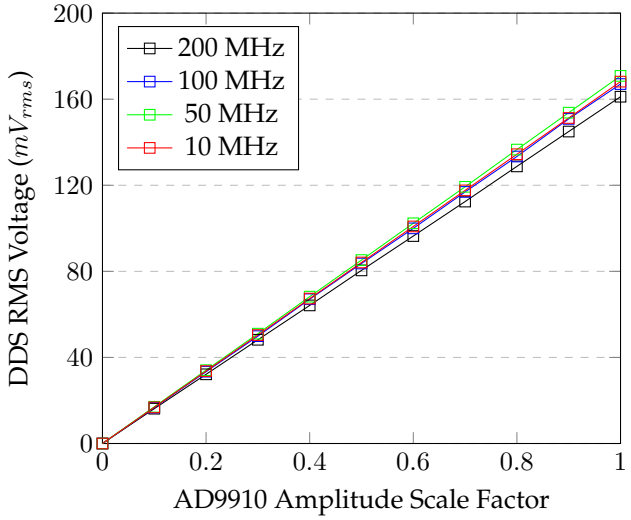


Figure 5: RMS voltage, 15dB attenuation

The ideal RMS voltage is described by the linear function $V_{\text{rms,ideal}}(\text{ASF}) = \frac{V_{\text{rms}}(0.1)}{0.1} * \text{ASF}$. The measured RMS voltage divided by the full scale ideal RMS voltage (i.e. $V_{\text{rms,ideal}}(1)$) is shown below.

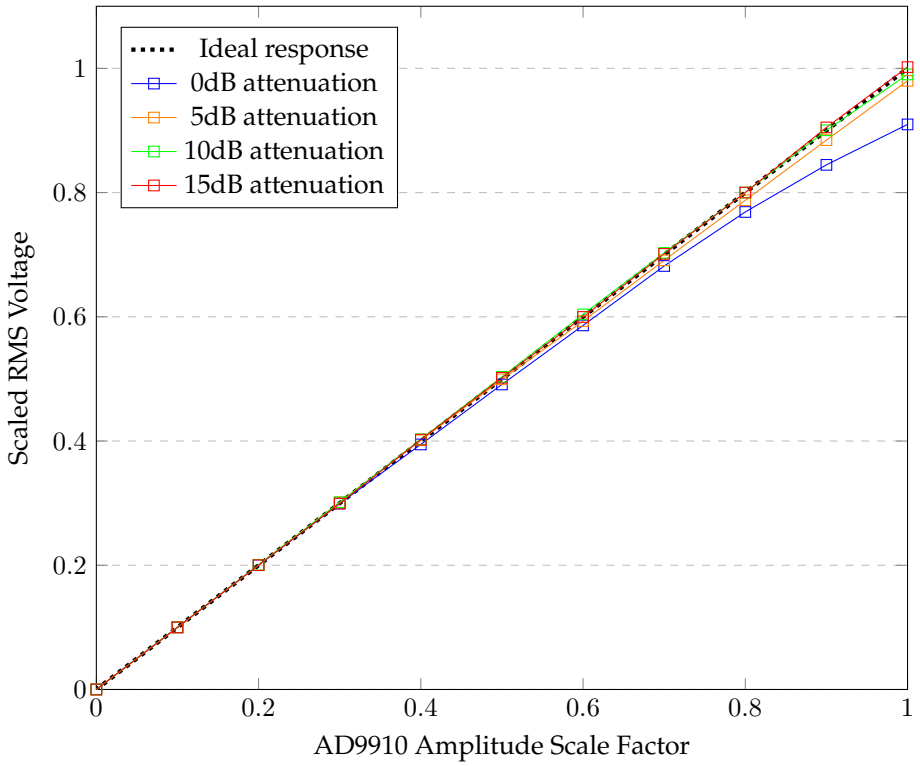


Figure 6: RMS voltage scaled by ideal voltage at ASF=1, 100 MHz

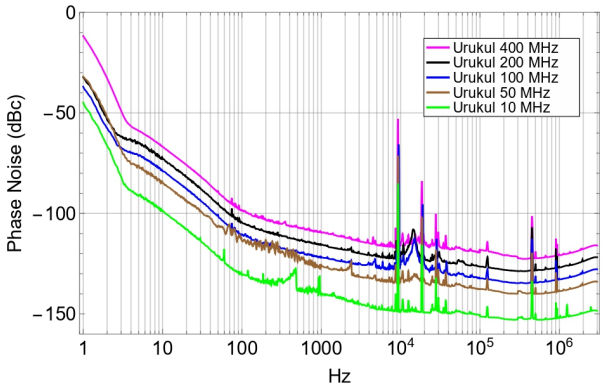


Figure 7: Phase noise of Urukul clocked by internal oscillator

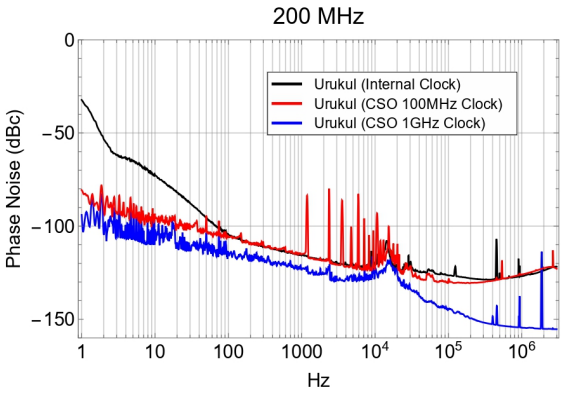


Figure 8: Phase noise of 200 MHz DDS Output

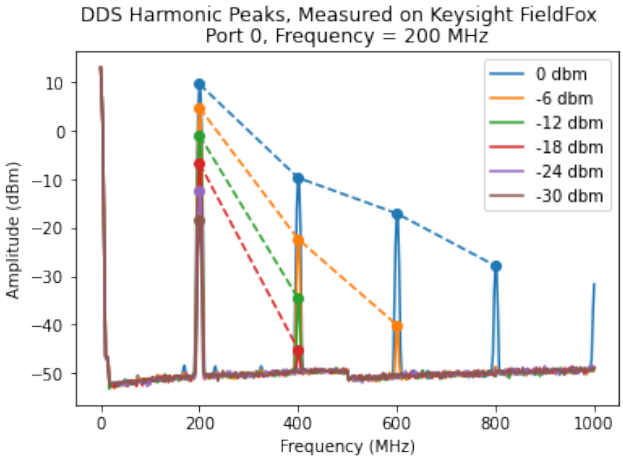


Figure 9: Harmonic content of 200 MHz DDS Output[8]

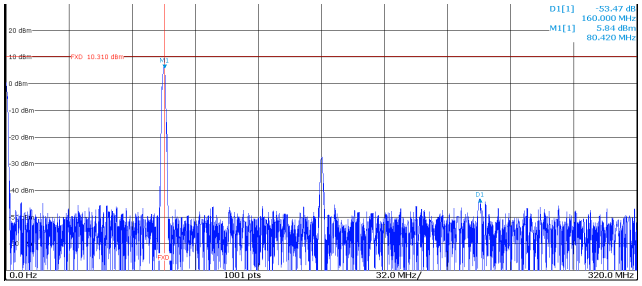


Figure 10: Harmonic content of 80 MHz DDS Output (6 dBm)[6]

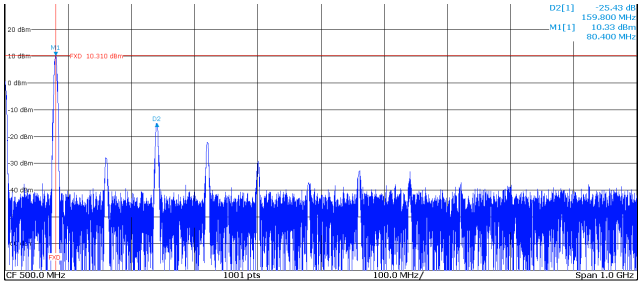


Figure 11: Harmonic content of 80 MHz DDS Output (10 dBm)[6]

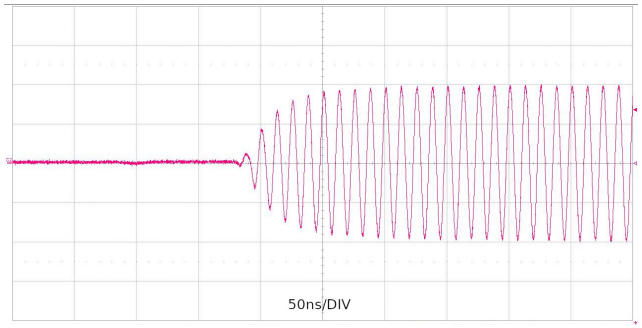


Figure 12: RF switch turn on transient[6]

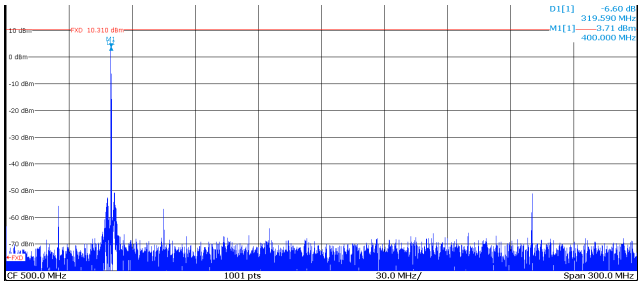


Figure 13: Nyquist rejection 400 MHz to 600 MHz[6]

[8] https://github.com/sinara-hw/Urukul/issues/64

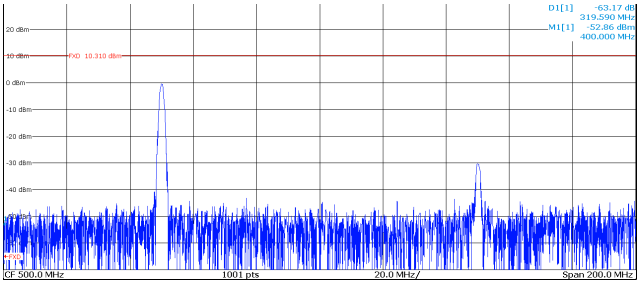


Figure 14: Nyquist rejection 450 MHz to 550 MHz[6]

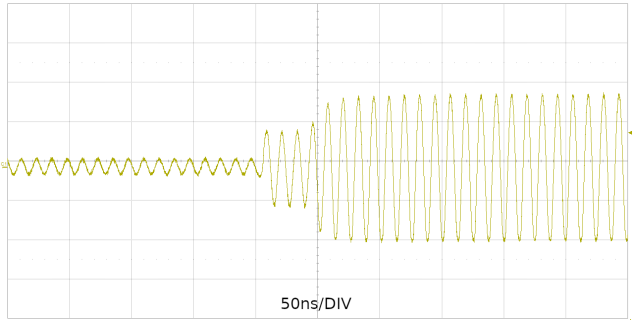


Figure 15: Attenuator step from 20 to 60 digital (16+4dB switch glitch)[6]

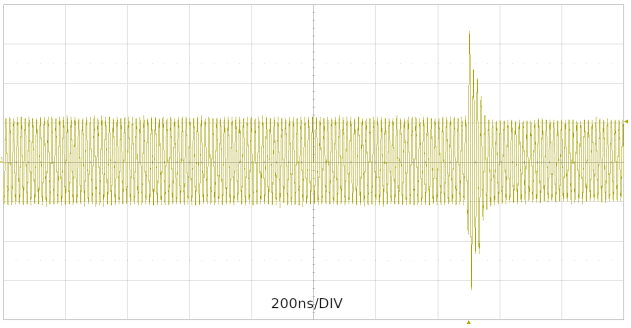


Figure 16: Attenuator step from 31 to 32 digital (major carry glitch)[6]

Configuring Operation Mode

Mode of operation is specified by a DIP switch. The DIP switch can be found at the top right corner of the card. The following table summarizes the required setting for each mode. ✓ indicates ON, while ✕ indicates OFF.

Table 8: DIP switch configurations

Mode	DIP Switch			
	1	2	3	4
Default	✕	✕	✕	✕
SU-Servo	✓	✓	✕	✕

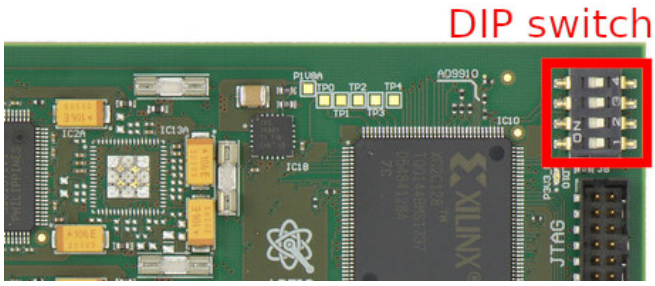


Figure 17: Position of DIP switch

Urukul Single-/Double-EEM Modes

4410/4412 DDS Urukul cards can operate with either a single or double EEM connections. When only EEM0 is connected, the card will act in single-EEM mode; when both EEM0 and EEM1 are connected, the card will act in double-EEM mode. 2-EEM mode when both EEM0 & EEM1 are connected. Double-EEM mode provides these additional features in comparison to single-EEM mode:

- **1 ns temporal resolution RF switches**
  Without EEM1, the only way to access the switches is through the CPLD, using SPI.
  With EEM1, RF switches can be controlled as a TTL output through the LVDS transceiver. 1 ns temporal resolution can then be achieved using the ARTIQ RTIO system.
- **SU-Servo (4410 DDS Urukul feature)**
  SU-Servo requires both EEM0 & EEM1 to allow the control of multiple DDS channels simultaneously using the QSPI interface.

ARTIQ Example Code

The sections below demonstrate simple usage scenarios of extensions on the ARTIQ control system. These extensions make use of the resources of the 4410/4412 DDS Urukul. They do not exhaustively demonstrate all the features of the ARTIQ system.

The full documentation for ARTIQ software and gateware, including the guide for its use, is available at https://m-labs.hk/artiq/manual/. Please consult the manual for details and reference material of the functions and structures used here.

10 MHz sinusoidal wave

Generates a 10MHz sinusoid from RF0 with full scale amplitude, attenuated by 6 dB. Both the CPLD and the DDS channels should be initialized. By default, AD9910 single-tone profiles are programmed to profile 7.

```
@kernel
def run(self):
    self.core.reset()
    self.cpld.init()
    self.dds0.init()
    self.dds0.cfg_sw(True)
    self.dds0.set_att(6.*dB)
    self.dds0.set(10*MHz)
```

If the synchronization feature of AD9910 is enabled, RF signal across different channels of the same Urukul can be synchronized. For example, phase-coherent RF signal can be produced on both channel 0 and channel 1 after configuring an appropriate phase mode.

```
@kernel
def run(self):
    self.core.reset()
    self.cpld.init()

    self.dds0.init()
    self.dds0.cfg_sw(True)
    self.dds0.set_phase_mode(PHASE_MODE_TRACKING)
    self.dds0.set_att(6.*dB)
    self.dds1.init()
    self.dds1.cfg_sw(True)
    self.dds1.set_phase_mode(PHASE_MODE_TRACKING)
    self.dds1.set_att(6.*dB)

    self.dds0.set(frequency=10*MHz, phase=0.0)
    self.dds1.set(frequency=10*MHz, phase=0.25)    # 0.25 turns phase offset
```

Note that the phase difference between the 2 channels might not be exactly 0.25 turns, but it is a constant. It can be negated by adjusting the `phase` parameter.

Periodic RF pulse (AD9910 Only)

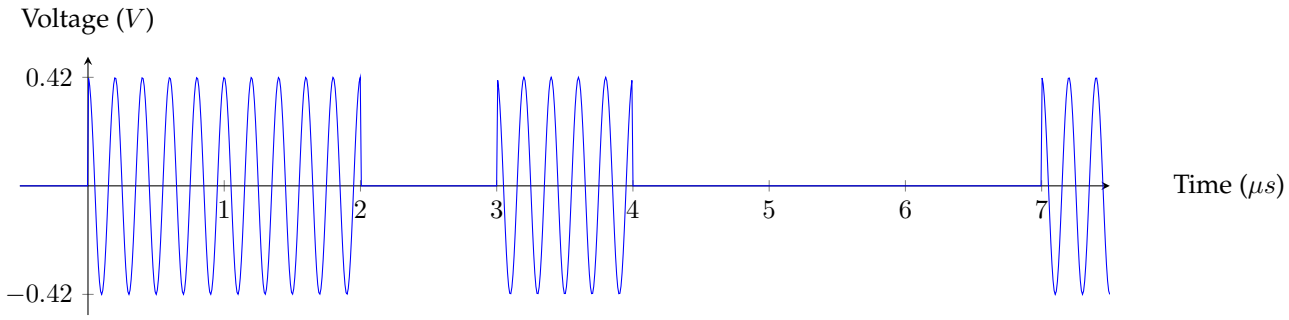
This example demonstrates that the RF signal can be modulated by amplitude using the RAM modulation feature of the AD9910. By default, RAM profiles are programmed to profile 0.

```
def prepare(self):
    self.amp = [0.0, 0.0, 0.0, 0.7, 0.0, 0.7, 0.7] # Reversed Order
    self.asf_ram = [0] * len(self.amp)

@kernel
def init_dds(self, dds):
    self.core.break_realtime()
    dds.init()
    dds.set_att(6.*dB)
    dds.cfg_sw(True)

@kernel
def configure_ram_mode(self, dds):
    self.core.break_realtime()
    dds.set_cfr1(ram_enable=0)
    self.cpld.io_update.pulse_mu(8)
    self.cpld.set_profile(0)     # Enable the corresponding RAM profile
                                 # Profile 0 is the default
    dds.set_profile_ram(start=0, end=len(self.asf_ram)-1,
        step=250, profile=0, mode=RAM_MODE_CONT_RAMPUP)
    self.cpld.io_update.pulse_mu(8)
    dds.amplitude_to_ram(self.amp, self.asf_ram)
    dds.write_ram(self.asf_ram)

    self.core.break_realtime()
    dds.set(frequency=5*MHz, ram_destination=RAM_DEST_ASF)
    # Pass osk_enable=1 to set_cfr1() if it is not an amplitude RAM
    dds.set_cfr1(ram_enable=1, ram_destination=RAM_DEST_ASF)

    self.cpld.io_update.pulse_mu(8)

@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.cpld.init()

    self.init_dds(self.dds0)
    self.configure_ram_mode(self.dds0)
```

The generated RF output of the above example consists of the following features in sequence:

1. A 5 MHz RF pulse for 2 microseconds.
2. No signal for 1 microseconds.
3. A 5 MHz RF pulse for 1 microseconds.
4. No signal for 3 microseconds.
5. Go back to item 1.

The expected waveform is plotted on the following figure. Note that phase of the RF pulses may drift gradually. Urukul was operated with a 50Ω termination to produce the waveform.

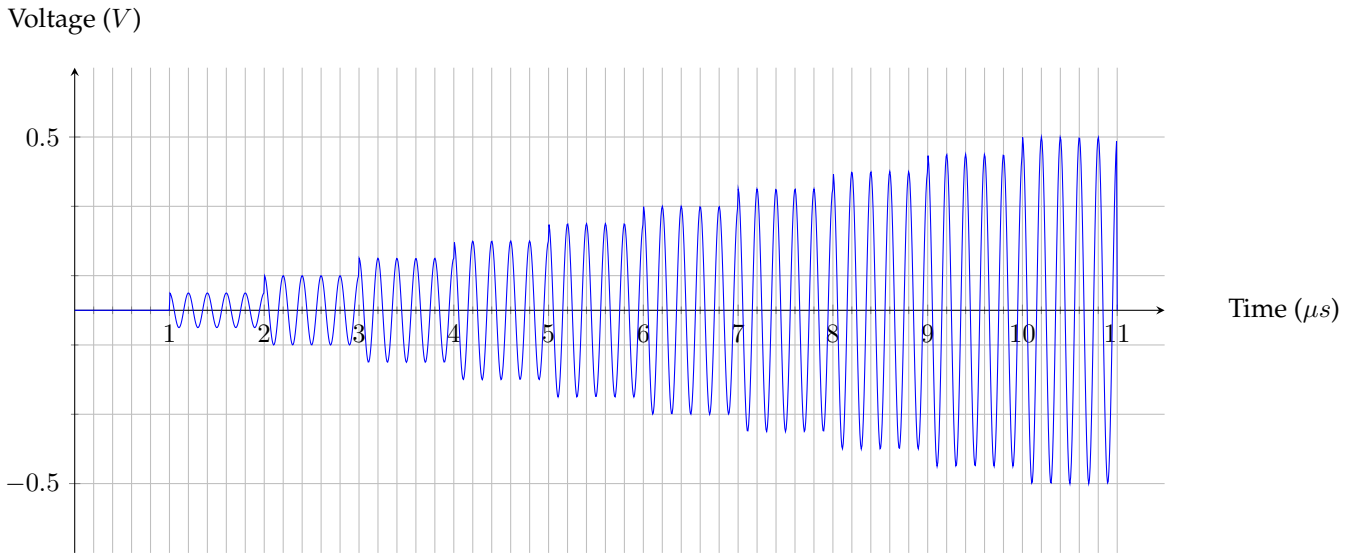


Simple amplitude ramp (AD9910 only)

An amplitude ramp of an RF signal can be generated by modifying the `self.amp` array in the previous example.

```
def prepare(self):
    # Reversed Order
    self.amp = [1.0, 0.9, 0.8, 0.7, 0.6, 0.5, 0.4, 0.3, 0.2, 0.1, 0.0]
    self.asf_ram = [0] * len(self.amp)
```

The generated RF output has an incrementing amplitude scale factor (ASF), increasing by 0.1 at every microsecond. Once the ASF reaches 1.0, it drops back to 0.0 at the next microsecond. The expected waveform over 1 cycle is plotted on the following figure. Note that phase of the RF pulses may drift gradually. Urukul was operated with a 50Ω termination to produce the waveform.



RAM synchronization (AD9910 only)

Multiple RAM channels can also be synchronized. Similar to the 10 MHz single-tone RF signals, specify `phase` when calling `dds.set()` in `configure_ram_mode`. For example, set phase to 0 for the channels (`phase=0.0`):

```
    dds.set(frequency=5*MHz, phase=0.0, ram_destination=RAM_DEST_ASF)
```

Then, replace the `run()` function with the following:

```
@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.cpld.init()

    self.init_dds(self.dds0)
    self.init_dds(self.dds1)
    self.dds0.set_phase_mode(PHASE_MODE_TRACKING)
    self.dds1.set_phase_mode(PHASE_MODE_TRACKING)

    self.configure_ram_mode(self.dds0)
    self.configure_ram_mode(self.dds1)
```

Two phase-coherent RF signal with the same waveform as the previous figure (from either RAM examples) should be generated.

Voltage-controlled DDS amplitude (SU-Servo only)

The SU-Servo feature can be enabled by integrating the 4410 DDS Urukul with a 5108 Sampler. Amplitude of the DDS output can be controlled by the ADC input of the Sampler through PI control, characterised by the following transfer function:

$$H(s) = k_p + \frac{k_i}{s + \frac{k_i}{g}}$$

In the following example, the amplitude of DDS is proportional to the ADC input from Sampler. First, initialize the RTIO, SU-Servo and its channel. Note that the programmable gain of the Sampler is $10^0 = 1$ and the input range is [-10V, 10V].

```
@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.suservo.init()
    self.suservo.set_pgia_mu(0, 0)  # unity gain
    self.suservo.cplds[0].set_att(0, 15.)
    self.suschannel0.set_y(profile=0, y=0.) # Clear integrator
```

Next, setup the PI control as an IIR filter. It has -1 proportional gain k_p and no integrator gain k_i.

```
    self.suschannel0.set_iir(
        profile=0,
        adc=0,          # take data from Sampler channel 0
        kp=-1.,         # -1 P gain
        ki=0./s,        # no integrator gain
        g=0.,           # no integrator gain limit
        delay=0.        # no IIR update delay after enabling
    )
```

Then, configure the DDS frequency to 10 MHz with 3V input offset. When input voltage ≥ offset voltage, the DDS output amplitude is 0.

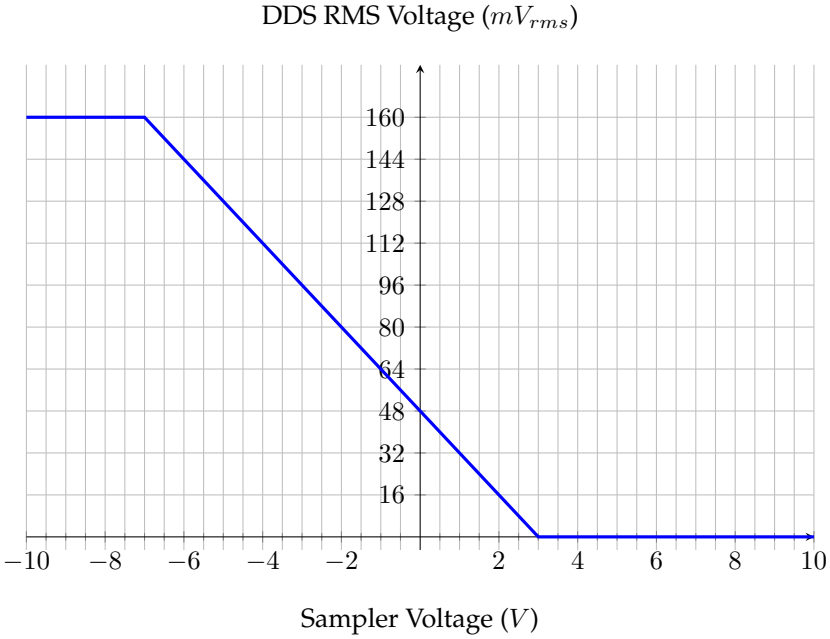
```
    self.suschannel0.set_dds(
        profile=0,
        offset=-.3,     # 3 V with above PGIA settings
        frequency=10*MHz,
        phase=0.)
```

SU-Servo encodes the ADC voltage in a linear scale [-1, 1]. Therefore, 3V is converted to 0.3. Note that the ASF of all DDS channels are capped at 1.0 and the amplitude clips when ADC input $\leq -7V$ with the above IIR filter.

Finally, enable the SU-Servo channel with the IIR filter programmed beforehand:

```
    self.suschannel0.set(en_out=1, en_iir=1, profile=0)
    self.suservo.set_config(enable=1)
```

A 10 MHz DDS signal is generated from the example above, with amplitude controllable by ADC. The RMS voltage of the DDS channel against the ADC voltage is plotted. The DDS channel is terminated with 50Ω.



DDS signal should be attenuated. High output power affects the linearity due to the 1 dB compression point of the amplifier at 13 dBm output power. 15 dB attenuation at the digital attenuator was applied in this example.

Ordering Information

To order, please visit https://m-labs.hk and choose 4410/4412 DDS Urukul in the ARTIQ/Sinara hardware selection tool. Cards can be ordered as part of a fully-featured ARTIQ/Sinara crate or standalone through the 'Spare cards' option. Otherwise, orders can also be made by writing directly to mailto:sales@m-labs.hk.