ARTIQ Sinara

5108 ADC Sampler

Features

- 8-channel ADC
- 16-bits resolution
- 1.5 MSPS simultaneously on all channels
- Full scale input voltage, ±10mV to ±10V
- BNC connector
- SMA breakout with 5528 SMA-IDC adapter

Applications

- Sample intermediate-frequency (IF) waveform
- Monitor laser power with a photodiode
- Synchronize laser frequencies with a phase frequency detector
- Form a laser intensity servo with 4410 Urukul

General Description

The 5108 ADC Sampler is a 8hp EEM module, part of the ARTIQ/Sinara family. It adds analog-digital converting capabilities to carrier cards such as 1124 Kasli and 1125 Kasli-SoC.

It provides eight analog-to-digital channels, exposed by eight BNC connectors. Each channel supports input voltage ranges from ±10mV to ±10V. All channels can be sampled simultaneously. Channels can broken out to SMA by adding a 5528 SMA-IDC card.

5108 ADC Sampler provides a sample rate of 1.5 MSPS. However, the sample rate in practice is typically limited by the use of ARTIQ-Python kernel code.

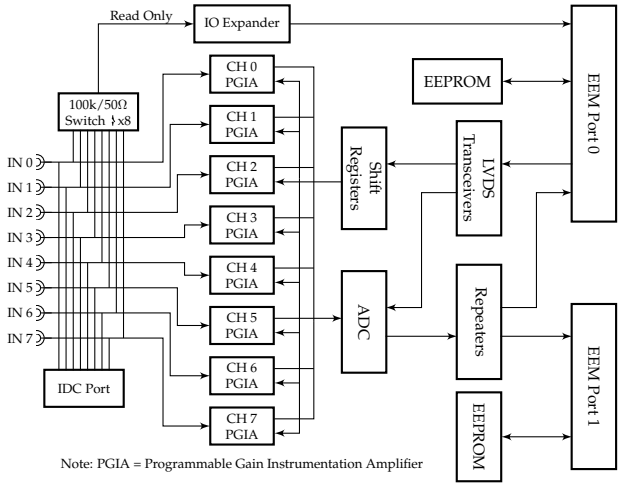


Figure 1: Simplified Block Diagram

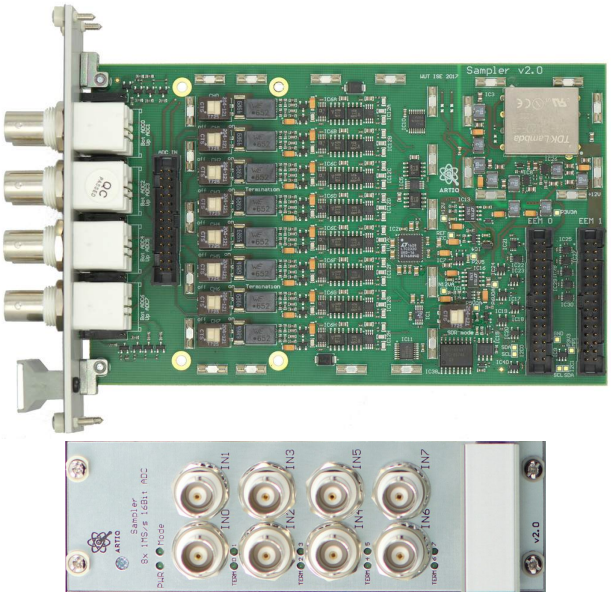


Figure 2: Sampler card and front panel

Source

5108 ADC Sampler, like all the Sinara hardware family, is open-source hardware, and design files (schematics, PCB layouts, BOMs) can be found in detail at the repository https://github.com/sinara-hw/Sampler.

Electrical Specifications

Table 1: Input Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
Input voltage	-10		10	V	1x gain, termination off*
	-1		1	V	10x gain
	-100		100	mV	100x gain
	-10		10	mV	1000x gain
DC Input signal impedance		100 kΩ			Termination off
		50 Ω			Termination on
Resolution		16 bits			

*With the 50Ω termination enabled, the input voltage magnitude must not exceed 5V.

The electrical characteristics are based on various test results[1, 2, 3].

Table 2: Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Conditions / Comments
-6dB bandwidth[3]					See bandwidth plots
		200		kHz	1x/10x/100x gain
		90		kHz	1000x gain
Noise[3]					83.33 kHz sampling rate
1x gain		1.78		LSB RMS	Termination on
		1.75		LSB RMS	Termination off
10x gain		1.84		LSB RMS	Termination on
		3.09		LSB RMS	Termination off
100x gain		3.47		LSB RMS	Termination on
		26.02		LSB RMS	Termination off
1000x gain		13.87		LSB RMS	Termination on
		206.3		LSB RMS	Termination off
DC cross-talk[1]			-96	dB	1x gain

[1] https://github.com/sinara-hw/sinara/issues/226
[2] https://github.com/sinara-hw/sinara/issues/489
[3] https://github.com/sinara-hw/Sampler/issues/2

Table 3: Electrical Characteristics (cont.)

Parameter	Min.	Typ.	Max.	Unit	Conditions / Comments
Second-order harmonics[1]					25 kHz input, termination on, 1x gain
		-51		dBc	0.1 V_{pp} (-48dBFS), limited by ADC (-100dBFS)
		-69		dBc	1 V_{pp} (-28dBFS)
		-58.8		dBc	10 V_{pp} (-8dBFS)
Common-mode rejection ratio[1]					2 V_{pp} sine wave as CM input, termination on
1x gain			-98	dB	$f = 0.01, 0.1, 1$ kHz
		-87		dB	$f = 10$ kHz
		-55		dB	$f = 100$ kHz
		-83		dB	$f = 1$ MHz
		-85		dB	$f = 10$ MHz
100x gain			-118	dB	$f = 0.01$ kHz
		-98		dB	$f = 0.1$ kHz
		-88		dB	$f = 1$ kHz
		-70		dB	$f = 10$ kHz
		-50		dB	$f = 100$ kHz
		-80		dB	$f = 1$ MHz
			-118	dB	$f = 10$ MHz

Channel crosstalk

Crosstalk between ADC channels of 5108 ADC Sampler is shown below[2].

A 10 V_{pp} signal was used as the input. The aggressor channel always has 1x gain. All channels have 50 Ω termination enabled.

Data was acquired by taking 512 samples at 80 kHz sampling rate 20 times to average out the FFT.

Table 4: Crosstalk with 35 kHz input frequency, 1000x gain on victim

Aggressor	Crosstalk (dB) on Victim Channels							
	0	1	2	3	4	5	6	7
Channel 0	0.00	-114.90	-129.35	-131.54	-132.19	-142.56	-145.39	-159.98

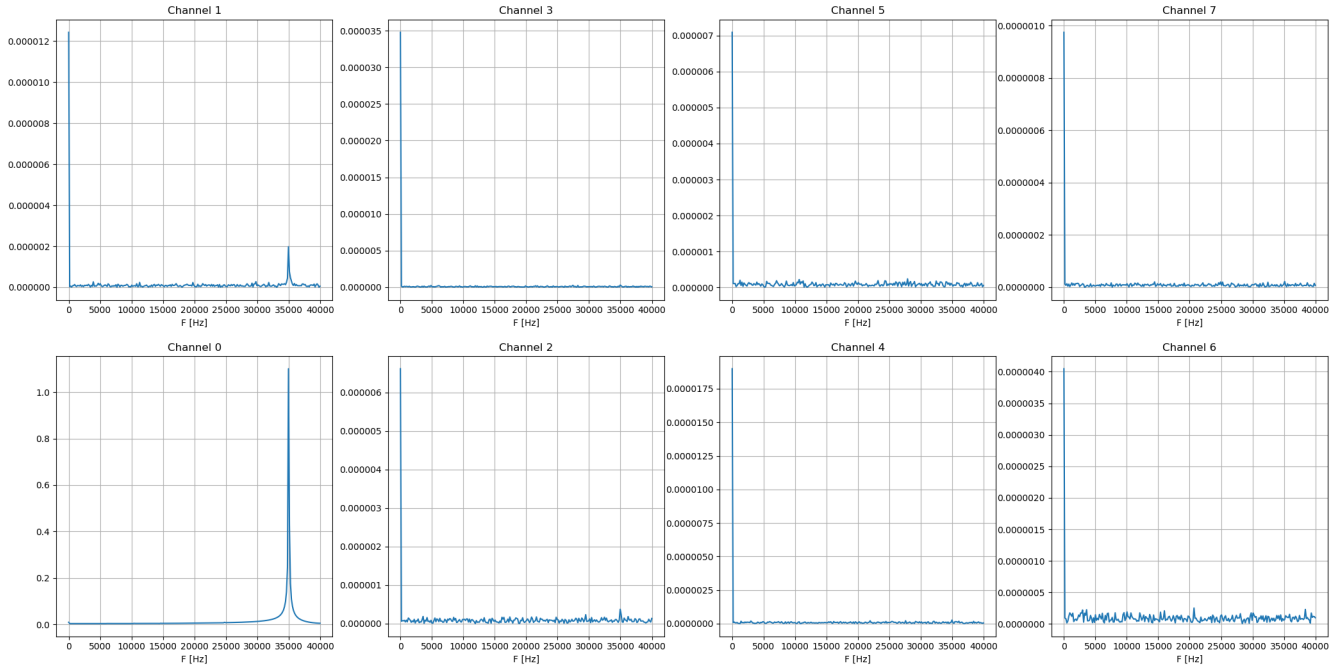


Figure 3: Crosstalk with 35 kHz input frequency, 1000x gain on victim, channel 0 as the aggressor

Table 5: Crosstalk with 300 kHz input frequency, 1000x gain on victim

Aggressor	Crosstalk (dB) on Victim Channels							
	0	1	2	3	4	5	6	7
Channel 0	0.00	-109.18	-123.94	-128.46	-131.11	-134.45	-135.62	-158.51
Channel 1	-112.90	0.00	-114.98	-124.11	-131.40	-142.61	-145.94	-168.51
Channel 2	-123.27	-112.58	0.00	-111.17	-121.46	-129.97	-137.31	-163.77
Channel 3	-140.61	-125.20	-114.49	0.00	-111.84	-125.10	-133.74	-164.55
Channel 4	-140.12	-131.07	-124.30	-112.65	0.00	-109.22	-124.71	-160.22
Channel 5	-140.33	-135.77	-134.42	-126.34	-116.35	0.00	-118.40	-156.63
Channel 6	-142.39	-139.25	-138.51	-134.73	-125.00	-108.91	0.00	-146.29
Channel 7	-145.06	-138.97	-144.31	-139.50	-135.50	-120.62	-114.28	0.00

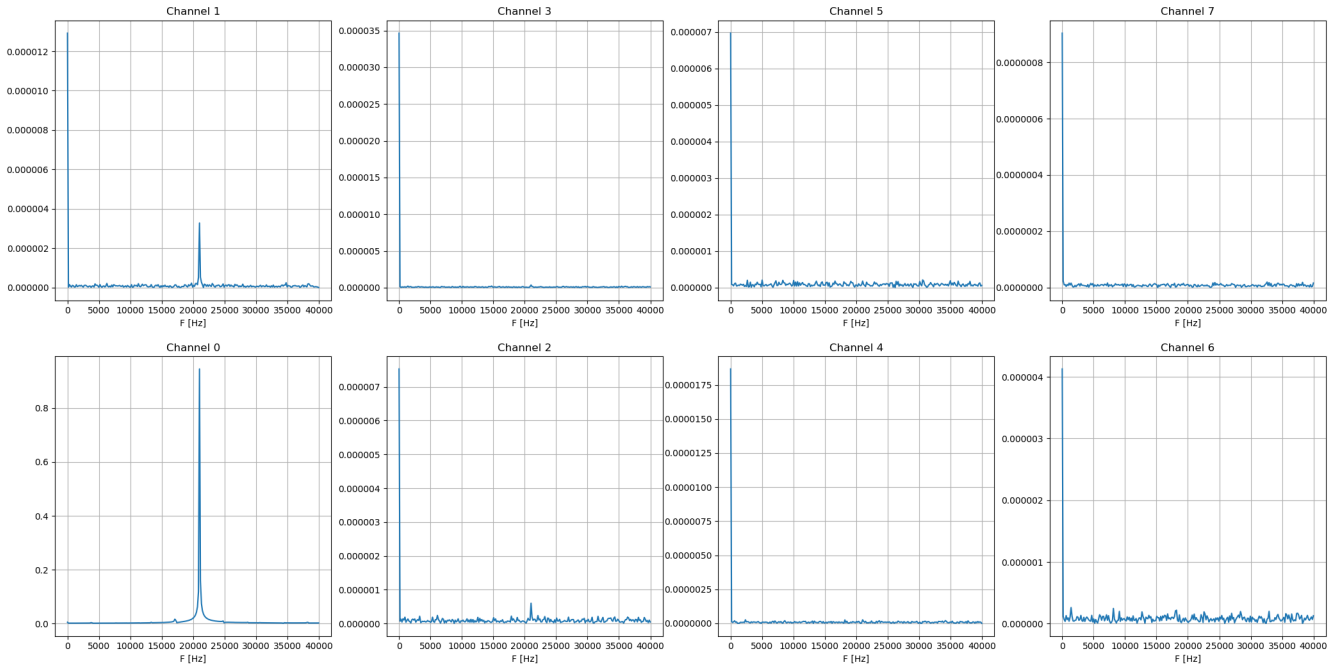


Figure 4: Crosstalk with 300 kHz input frequency, 1000x gain on victim, channel 0 as the aggressor

Table 6: Crosstalk with 300 kHz input frequency, 1x gain on victim

Aggressor	**Crosstalk (dB) on Victim Channels**							
	0	1	2	3	4	5	6	7
Channel 0	0.00	-84.36	-100.65	-100.16	-102.72	-93.51	-96.23	-105.70
Channel 1	-91.95	0.00	-87.47	-104.87	-115.80	-99.91	-101.55	-106.71
Channel 2	-109.04	-86.28	0.00	-88.78	-96.81	-95.41	-108.53	-109.23
Channel 3	-101.31	-97.47	-92.72	0.00	-88.65	-96.58	-100.80	-97.46
Channel 4	-101.27	-95.18	-97.16	-88.29	0.00	-87.26	-99.11	-100.12
Channel 5	-103.41	-102.10	-101.54	-104.59	-99.87	0.00	-89.34	-102.49
Channel 6	-104.62	-104.64	-103.39	-101.73	-104.08	-87.61	0.00	-88.34
Channel 7	-100.67	-99.20	-97.34	-95.48	-102.93	-113.76	-92.80	0.00

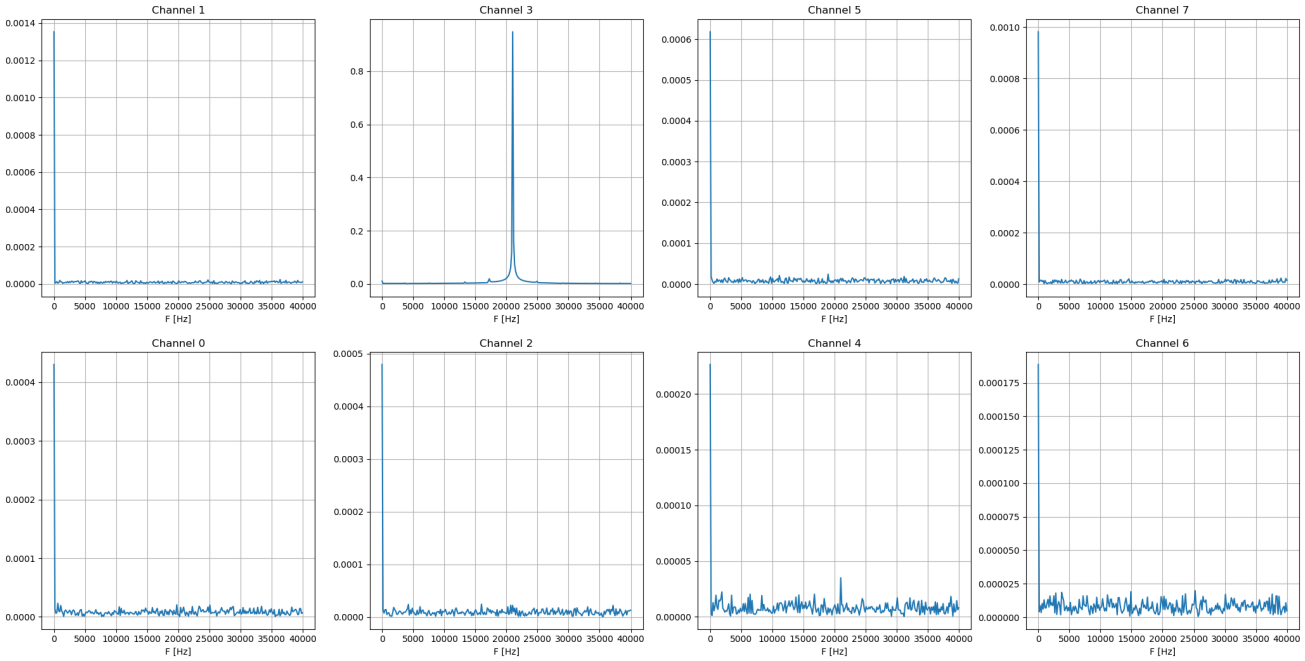


Figure 5: Crosstalk with 300 kHz input frequency, 1x gain on victim, channel 3 as the aggressor

Bandwidth

Bandwidth of small signal and large signal input is shown below[3]. The setup is as follows:

1. 10k samples, sampled at 79.37 kHz
2. Driven by sinusoid from Keysight 33500B generator; sampled using channel 7 without termination
3. Small signal measured using $2V_{pp}$/gain; large signal measured using $15V_{pp}$/gain

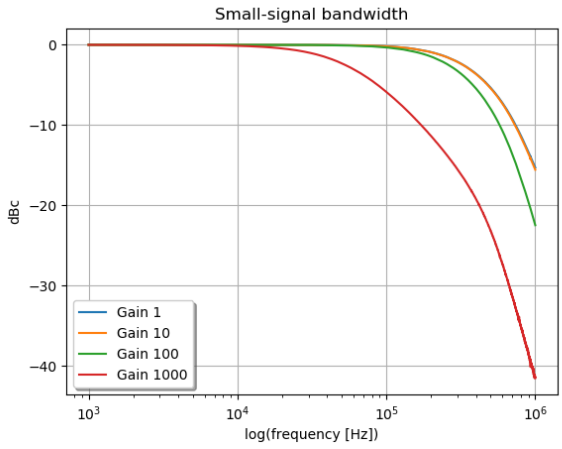


Figure 6: Small signal bandwidth

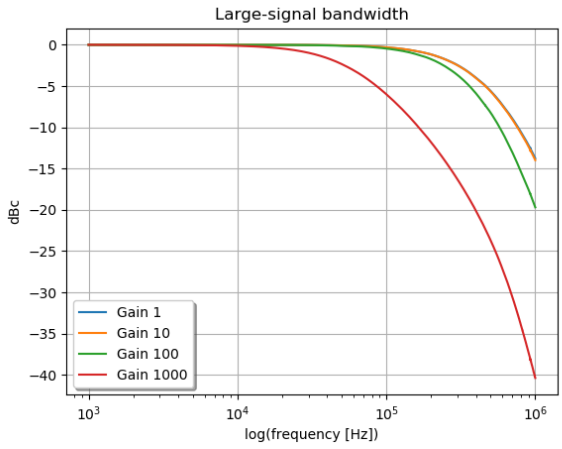


Figure 7: Large signal bandwidth

Configuring Termination

The input termination must be configured by setting physical switches on the board. The termination switches are found at the middle left part of the card are by-channel. Switching the termination switches on adds a 50Ω termination between the differential input signals.

Regardless of switch configurations, the differential input signals are separately terminated with 100kΩ to the PCB ground.

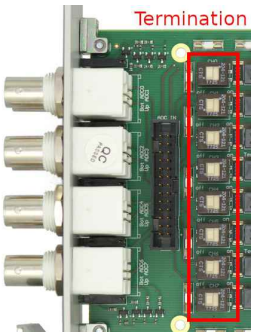


Figure 8: Position of switches

Example ARTIQ Code

The sections below demonstrate simple usage scenarios of extensions on the ARTIQ control system. These extensions make use of the resources of the 5108 ADC Sampler. They do not exhaustively demonstrate all the features of the ARTIQ system.

The full documentation for ARTIQ software and gateware, including the guide for its use, is available at https://m-labs.hk/artiq/manual/. Please consult the manual for details and reference material of the functions and structures used here.

Get input voltage

The following example initializes the Sampler card with 1x gain on all ADC channels. At the end all ADC channels are sampled.

```
def prepare(self):
    self.smp = [0.0]*8

@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.sampler.init()
    delay(5*ms)
    for i in range(8):
        self.sampler.set_gain_mu(i, 0)
        delay(100*us)
    self.sampler.sample(self.smp)
```

Voltage-controlled DDS amplitude (SU-Servo only)

SU-Servo configuration can be enabled by integrating the 5108 ADC Sampler with 4410 DDS Urukul. Amplitude of the DDS output can be controlled by the ADC input of the Sampler through PI control, characterised by the following transfer function:

$$H(s) = k_p + \frac{k_i}{s + \frac{k_i}{g}}$$

In the following example, the amplitude of DDS is proportional to the ADC input from Sampler.

First, initialize the RTIO, SU-Servo and its channel with 1x gain.

```
@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.suservo.init()
    self.suservo.set_pgia_mu(0, 0)  # unity gain
    self.suservo.cplds[0].set_att(0, 15.)
    self.suschannel0.set_y(profile=0, y=0.) # Clear integrator
```

Next, set up the PI control as an IIR filter. It has -1 proportional gain k_p and no integrator gain k_i.

```
    self.suschannel0.set_iir(
        profile=0,
        adc=0,          # take data from Sampler channel 0
        kp=-1.,         # -1 P gain
        ki=0./s,        # no integrator gain
        g=0.,           # no integrator gain limit
        delay=0.        # no IIR update delay after enabling
    )
```

Then, configure the DDS frequency to 10 MHz with 3V input offset. When input voltage $\geq$ offset voltage, the DDS output amplitude is 0.

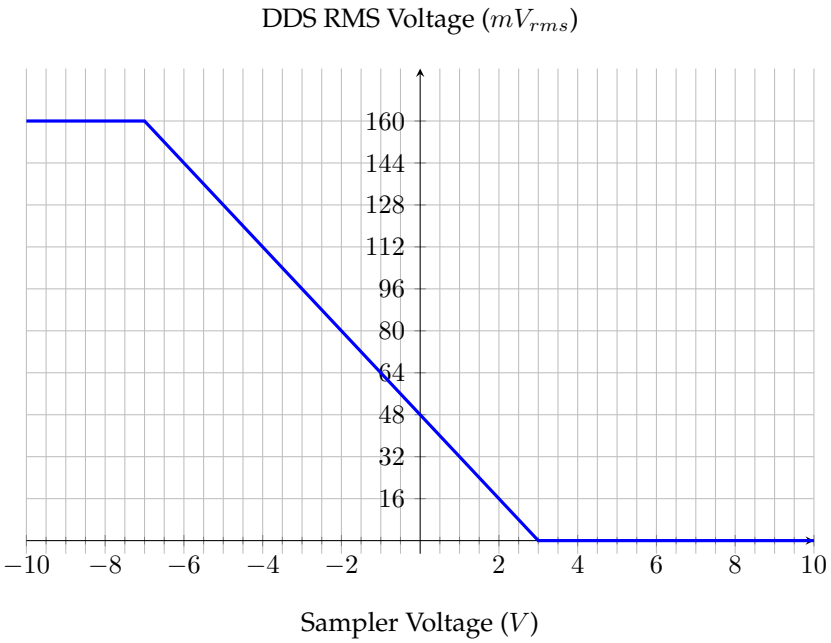
```
    self.suschannel0.set_dds(
        profile=0,
        offset=-.3,     # 3 V with above PGIA settings
        frequency=10*MHz,
        phase=0.)
```

SU-Servo encodes the ADC voltage in a linear scale [-1, 1]. Therefore, 3V is converted to 0.3. Note that the ASF of all DDS channels are capped at 1.0; the amplitude clips when ADC input $\leq -7V$ with the above IIR filter.

Finally, enable the SU-Servo channel with the IIR filter programmed beforehand:

```
    self.suschannel0.set(en_out=1, en_iir=1, profile=0)
    self.suservo.set_config(enable=1)
```

A 10 MHz DDS signal is generated from the example above, with amplitude controllable by ADC. The RMS voltage of the DDS channel against the ADC voltage is plotted. The DDS channel is terminated with 50Ω.



DDS signal should be attenuated. High output power affects the linearity due to the 1 dB compression point of the amplifier at 13 dBm output power. 15 dB attenuation at the digital attenuator was applied in this example.

Ordering Information

To order, please visit https://m-labs.hk and choose 5108 ADC Sampler in the ARTIQ/Sinara hardware selection tool. Cards can be ordered as part of a fully-featured ARTIQ/Sinara crate or standalone through the 'Spare cards' option. Otherwise, orders can also be made by writing directly to mailto:sales@m-labs.hk.

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