4456 Synthesizer Mirny

Features

- 4-channel VCO/PLL
- Output frequency ranges from 53 MHz to >4 GHz
- Up to 13.6 GHz with Almazny mezzanine
- Higher frequency resolution than Urukul
- Lower jitter and phase noise
- Large frequency changes take several milliseconds

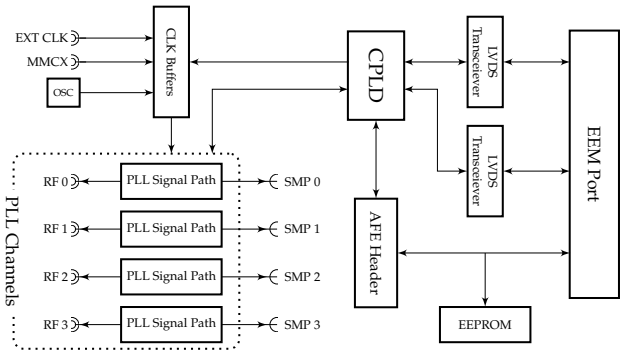

Figure 1: Simplified Block Diagram

Applications

- Low-noise microwave source
- Quantum state control
- Driving acousto/electro-optic modulators

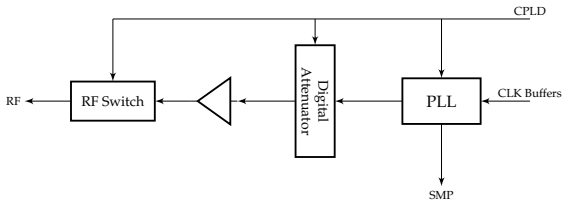

Figure 2: Simplified PLL Signal Path

General Description

The 4456 Synthesizer Mirny card is a 4hp EEM module, part of the ARTIQ/Sinara family. It adds microwave generation capabilities to carrier cards such as 1124 Kasli and 1125 Kasli-SoC.

It provides 4 channels of PLL frequency synthesis. Output frequencies from 53 MHz to >4 GHz are supported.The range can be expanded up to 13.6 GHz with the Almazny mezzanine (4467 HF Synthesizer).

Each channel can be attenuated from 0 to -31.5 dB by a digital attenuator. RF switches on each channel provides at least 50 dB isolation.

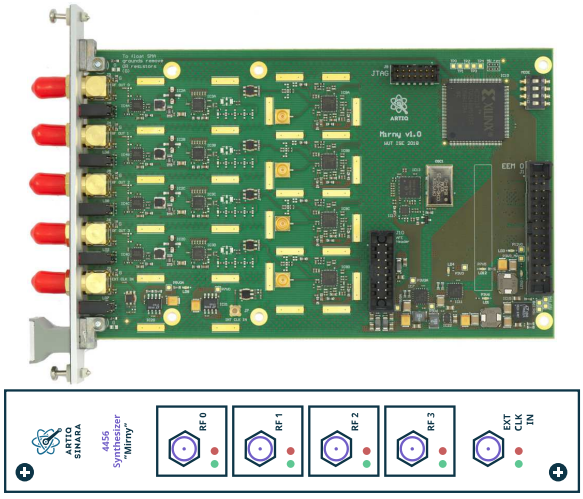

Figure 3: Mirny card and front panel

Source

4456 Synthesizer Mirny, like all the Sinara hardware family, is open-source hardware, and design files (schematics, PCB layouts, BOMs) can be found in detail at the repository https://github.com/sinara-hw/mirny.

Electrical Specifications

Specifications of parameters are based on the datasheets of the PLL IC (ADF5356[1]), clock buffer IC (Si53340-B-GM[2]), and digital attenuator IC (HMC542BLP4E[3]). Test results are from Krzysztof Belewicz's thesis. "Microwave synthesizer for driving ion traps in quantum computing"[4].

Table 1: Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Conditions
Clock input					
Frequency[1]	10		250	MHz	Single-ended clock input (PLL config.)
	10		600	MHz	Differential clock input (PLL config.)
Differential input swing[2]	0.11		1.55	V_{p-p}	

Table 2: Output Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
Frequency	53.125		4000	MHz	
Digital attenuation[3]	-31.5		0	dB	
Resolution					
Frequency[1]		52 bits			
Phase offset[1]		24 bits			
Digital attenuation[3]		0.5 dB			

[1] https://www.analog.com/media/en/technical-documentation/data-sheets/ADF5356.pdf
[2] https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/si5334x-datasheet.pdf
[3] https://www.analog.com/media/en/technical-documentation/data-sheets/hmc542b.pdf
[4] https://m-labs.hk/Krzysztof_Belewicz_V1.1.pdf

Phase noise performance of Mirny was tested using the ADF4351 evaluation kit[4]. The SPI signal was driven by the evaluation kit, converted into LVDS signal by propagating through the DIO-tester card, finally arriving at the Mirny card. Mirny was then connected to the RSA5100A spectrum analyzer for measurement.

Noise response spike can be improved by inserting an additional common-mode choke between the power supply and Mirny; note that this common-mode choke is not present on the card itself. The following is a comparison between the two setups at 1 GHz output:

- Red: Before any modifications
- Blue: CM choke added with an 100 µF capacitor after the CM choke

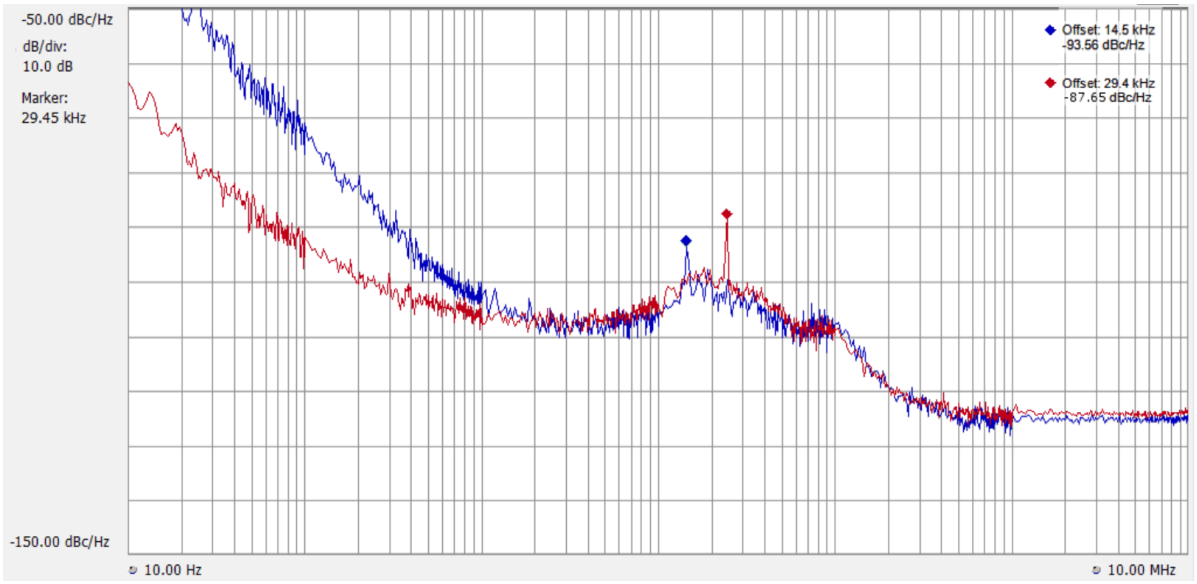

Figure 4: Phase noise measurement at 1 GHz

Phase noise at different output frequencies is then measured:

Table 3: Phase noise performance

Output frequency	Phase noise (dBc/Hz) at carrier offset				
	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
125 MHz	-114	-116	-115	-132	-133
500 MHz	-107	-129	-111	-130	-132
1 GHz	-102	-106	-107	-125	-133
2 GHz	-102	-98	-104	-123	-124
3.5 GHz	-96	-101	-103	-127	-128

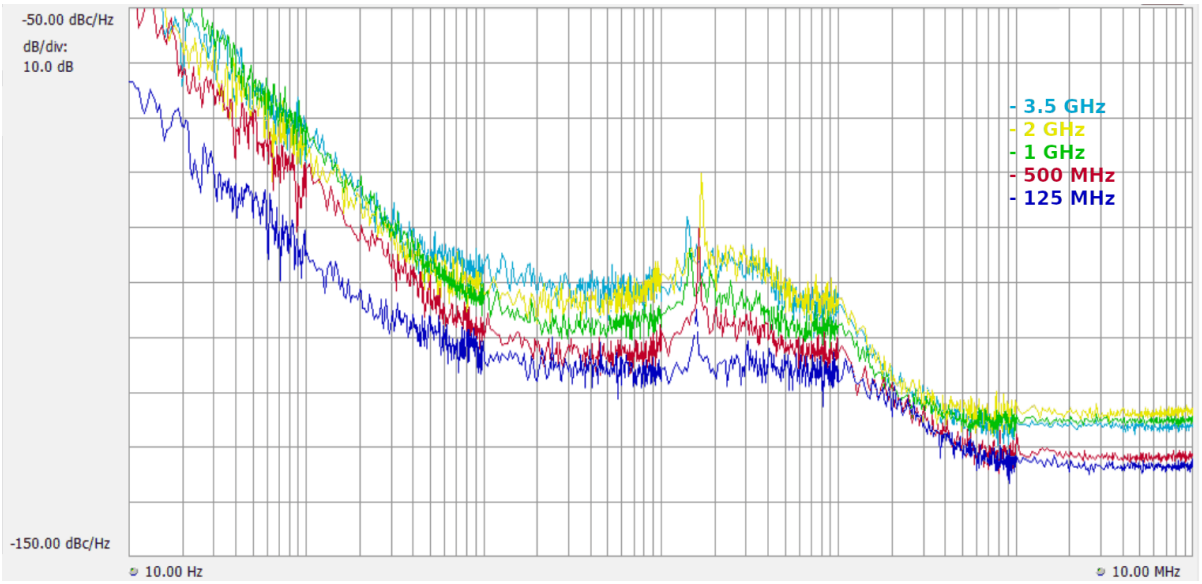

Figure 5: Phase noise measurement

Example ARTIQ Code

The sections below demonstrate simple usage scenarios of extensions on the ARTIQ control system. These extensions make use of the resources of the 4456 Synthesizer Mirny. They do not exhaustively demonstrate all the features of the ARTIQ system.

The full documentation for ARTIQ software and gateware, including guides for their use, is available at https://m-labs.hk/artiq/manual/. Please consult the manual for details and reference material of the functions and structures used here.

1 GHz sinusoidal wave

Generates a 1 GHz sinusoid from RF0 with full scale amplitude, attenuated by 12 dB. Both the CPLD and the PLL channels should be initialized.

```
@kernel
def init_mirny(self):
    self.core.reset()
    self.cpld.init()
    self.pll0.init()
    self.pll0.set_frequency(1*GHz)
    self.pll0.set_att(12*dB)
    self.pll0.sw.on()
```

ADF5356 power control

Output power can be controlled be configuring the PLL channels individually in addition to the digital attenuators. After initialization of the PLL channel (ADF5356), the following line of code can change the output power level:

```
    self.pll0.set_output_power_mu(0)
```

The parameter corresponds to a specific change of output power according to the following table[1].

Table 4: Power changes from ADF5356

Parameter	Power
0	-4 dBm
1	-1 dBm
2	+2 dBm
3	+5 dBm

ADF5356 gives +5 dBm by default. The stored parameter in ADF5356 can be read using the following line"

```
print(self.pll0.output_power_mu())
```

Periodic 100µs pulses

The output can be toggled on and off periodically using the RF switches. The following code emits a 100µs pulse in every millisecond. A microwave signal should be programmed in prior (such as the 1 GHz wave example).

```
while True:
    self.pll0.sw.pulse(100*us)
    delay(900*us)
```

Ordering Information

To order, please visit https://m-labs.hk and choose 4456 Synthesizer Mirny in the ARTIQ/Sinara hardware selection tool. Cards can be ordered as part of a fully-featured ARTIQ/Sinara crate or standalone through the 'Spare cards' option. Otherwise, orders can also be made by writing directly to mailto:sales@m-labs.hk.