5432 DAC Zotino

Features

- 32-channel DAC
- 16-bits resolution
- 1 MSPS shared between all channels
- Output voltage ±10V
- HD68 connector
- Can be broken out to BNC/SMA/MCX

Applications

- Controlling setpoints of PID controllers for laser power stabilization
- Low-frequency arbitrary waveform generation
- Driving DC electrodes in ion traps

General Description

The 5432 Zotino is a 4hp EEM module and part of the ARTIQ/Sinara family. It adds digital-analog conversion capabilities to carrier cards such as 1124 Kasli and 1125 Kasli-SoC.

It provides four groups of eight analog channels each, exposed by one HD68 connector. Each channel supports output voltage from -10 V to 10 V. All channels can be updated simultaneously. Channels can broken out to BNC, SMA or MCX by adding external 5518 BNC-IDC, 5528 SMA-IDC or 5538 MCX-IDC cards.

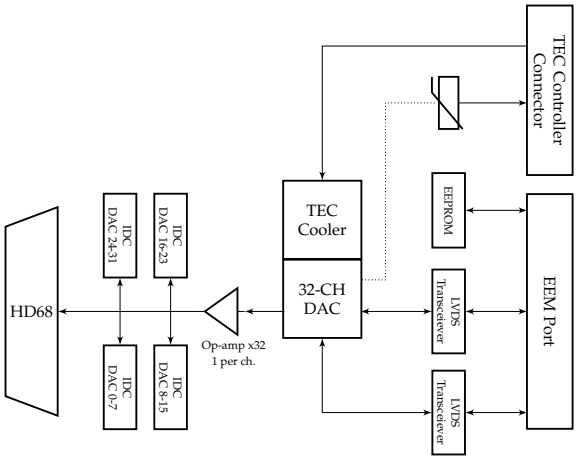


Figure 1: Simplified Block Diagram

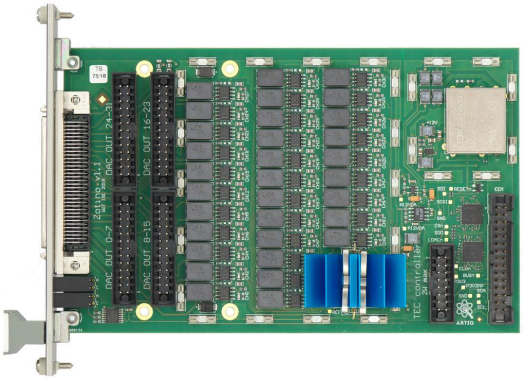


Figure 2: Zotino card photograph

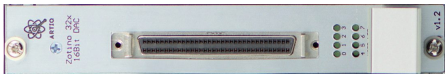


Figure 3: Zotino front panel

Source

5432 DAC Zotino, like all the Sinara hardware family, is open-source hardware, and design files (schematics, PCB layouts, BOMs) can be found in detail at the repository https://github.com/sinara-hw/Zotino/.

Electrical Specifications

These specifications are based on the datasheet of the DAC IC (AD5372BCPZ[1]), and various information from the Sinara wiki[2].

Table 1: Output Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
Output voltage	-10		10	V	
Output impedance[2]		470 Ω || 2.2nF			
Resolution[1]		16		bits	
3dB bandwidth[2]		75		kHz	
Power consumption[2]	3		8.7	W	

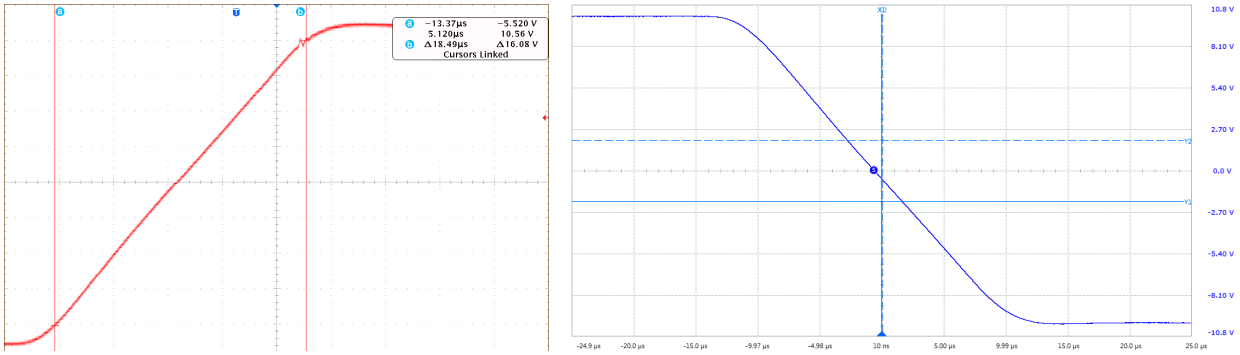
The following table records the cross-talk and transient behavior of Zotino[3]. In terms of output noise, measurements were made after a 15-cm IDC cable, IDC-SMA, 100 cm coax (∼50 pF), and 500 kΩ || 150 pF[4]. DAC output during noise measurement was 3.5 V.

Table 2: Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Conditions / Comments
DC cross-talk[3]		-116		dB	
Fall-time[3]		18.5		µs	10% to 90% fall-time
		25		µs	1% to 99% fall-time
Negative overshoot[3]		0.5%		-	
Rise-time[3]		30		µs	1% to 99% rise-time
Positive overshoot[3]		0.65%		-	
Output noise[4]					
@ 100 Hz		500		nV/rtHz	6.9 Hz bandwidth
@ 300 Hz		300		nV/rtHz	6.9 Hz bandwidth
@ 50 kHz		210		nV/rtHz	6.9 kHz bandwidth
@ 1 MHz		4.6		nV/rtHz	6.9 kHz bandwidth
> 4 MHz			1	nV/rtHz	6.9 kHz bandwidth

[1] https://www.analog.com/media/en/technical-documentation/data-sheets/AD5372_5373.pdf
[2] https://github.com/sinara-hw/Zotino/wiki
[3] https://github.com/sinara-hw/Zotino/issues/21
[4] https://github.com/sinara-hw/Zotino/issues/27

Step response was found by setting the DAC register to 0x0000 (-10V) or 0xFFFF (10V) and observing the waveform[3].



(a) Switching from -10V to +10V

(b) Switching from +10V to -10V

Figure 4: Step response

Far-end crosstalk was measured using the following setup[3]:

1. CH1 as aggressor, CH0 as victim
2. CH0, 2-7 terminated, CH 8-31 open
3. Aggressor signal from BNC passed through 15cm IDC26, 2m HD68-HD68 SCSI-3 shielded twisted pair, 15cm IDC26, converted back to BNC with adapters between all different cables and connectors.

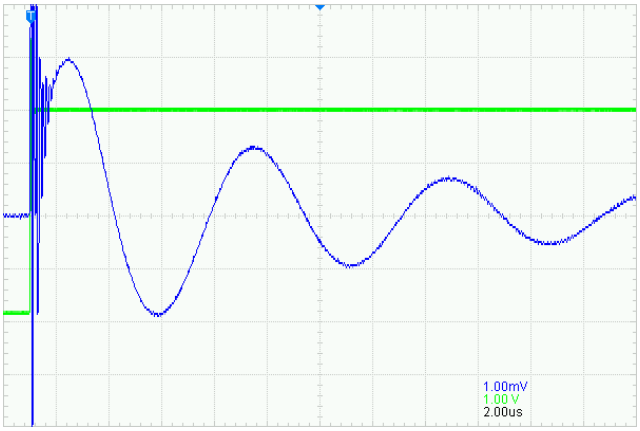


Figure 5: Step crosstalk

Example ARTIQ Code

The sections below demonstrate simple usage scenarios of extensions on the ARTIQ control system. These extensions make use of the resources of the 5432 DAC Zotino. They do not exhaustively demonstrate all the features of the ARTIQ system.

The full documentation for ARTIQ software and gateware, including guides for their use, is available at https://m-labs.hk/artiq/manual/. Please consult the manual for details and reference material of the functions and structures used here.

Setting output voltage

The following example initializes the Zotino card, then emits 1.0 V, 2.0 V, 3.0 V and 4.0 V at channels 0, 1, 2, and 3 respectively. Voltages of all 4 channels are updated simultaneously with the use of `set_dac()`.

```
def prepare(self):
    self.channels = [0, 1, 2, 3]
    self.voltages = [1.0, 2.0, 3.0, 4.0]

@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.zotino.init()

    delay(1*ms)
    self.zotino.set_dac(self.voltages, self.channels)
```

Triangular wave

Generates a triangular waveform at 10 Hz, 16 V peak-to-peak. Timing accuracy of the RTIO system can be demonstrated by the precision of the frequency.

Import `scipy.signal` and `numpy` modules to run this example.

```
def prepare(self):
    self.period = 0.1*s
    self.sample = 128
    t = numpy.linspace(0, 1, self.sample)
    self.voltages = 8*signal.sawtooth(2*numpy.pi*t, 0.5)
    self.interval = self.period/self.sample

@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.zotino.init()

    delay(1*ms)

    counter = 0
    while True:
        self.zotino.set_dac([self.voltages[counter]], [0])
        counter = (counter + 1) % self.sample
        delay(self.interval)
```

Ordering Information

To order, please visit https://m-labs.hk and choose 5432 DAC Zotino in the ARTIQ/Sinara hardware selection tool. Cards can be ordered as part of a fully-featured ARTIQ/Sinara crate or standalone through the 'Spare cards' option. Otherwise, orders can also be made by writing directly to mailto:sales@m-labs.hk.