Freescale Technology Forum

Design Innovation.

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Designing for DDR3 Memory on Freescale Microprocessors

FN110

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Introduction

- Customers are beginning to inquire and expect DDR3 support on their new product offerings, especially as the price cross-over point nears.
- The first device with DDR3 support is PowerQUICC® MPC8572.
- The first development system with DDR3 will be QorIQ™ P2020.
- As such, more and more FSL products are supporting DDR3 moving forward.
- In this session we will look at key distinctions between DDR3 vs. DDR1 and DDR2, with key emphasis placed on elements that are important to hardware and board design engineers.

DDR3 – Same Players

- Supported by all major memory vendors

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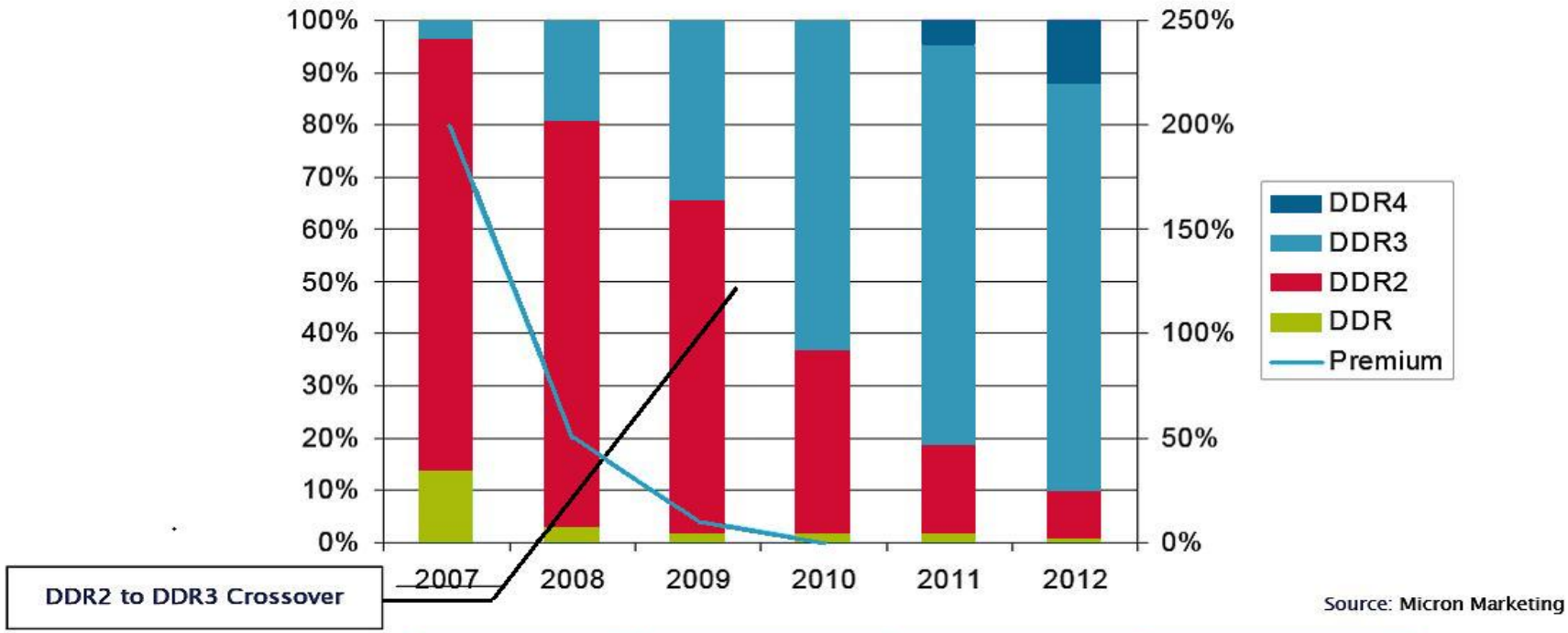
Cross-over in the Next 18-24 Months



Source: Micron Marketing

	2007	2008	2009	2010
DDR	14%	3%	2%	1%
DDR2	83%	78%	64%	33%
DDR3	3%	19%	34%	60%

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DDR SDRAM Highlights and Comparison

Feature/Category	DDR1	DDR2	DDR3
Package	TSOP	BGA only	BGA only
Densities	128 Mb -1 Gb	256 Mb – 4 Gb	512 Mb -8 Gb
Voltage	2.5V Core 2.5V I/O	1.8V Core 1.8V I/O	1.5V Core 1.5V I/O
I/O Signaling	SSTL_2	SSTL_18	SSTL_15
Internal Memory Banks	4	4 to 8	8
Data Rate	200-400 Mbps	400–800 Mbps	800–1600 Mbps
Termination	Motherboard termination to V_{TT} for all signals	On-die termination for data group. V_{TT} termination for address, command, and control	On-die termination for data group. V_{TT} termination for address, command, and control
Data Strobes	Single Ended	Differential or single	Differential

DDR SDRAM Highlights and Comparison (cont.)

Feature/Category	DDR1	DDR2	DDR3
Burst Length	BL= 2, 4, 8 (2-bit prefetch)	BL= 4, 8 (4-bit prefetch)	BL= 8 (Burst chop 4) (8-bit prefetch)
CL/tRCD/tRP	15 ns each	15 ns each	12 ns each
Master Reset	No	No	Yes
ODT (On-die termination)	No	Yes	Yes
Driver Calibration	No	Off-Chip (OCD)	On-Chip with ZQ pin (ZQ cal)
Write Leveling	No	No	Yes

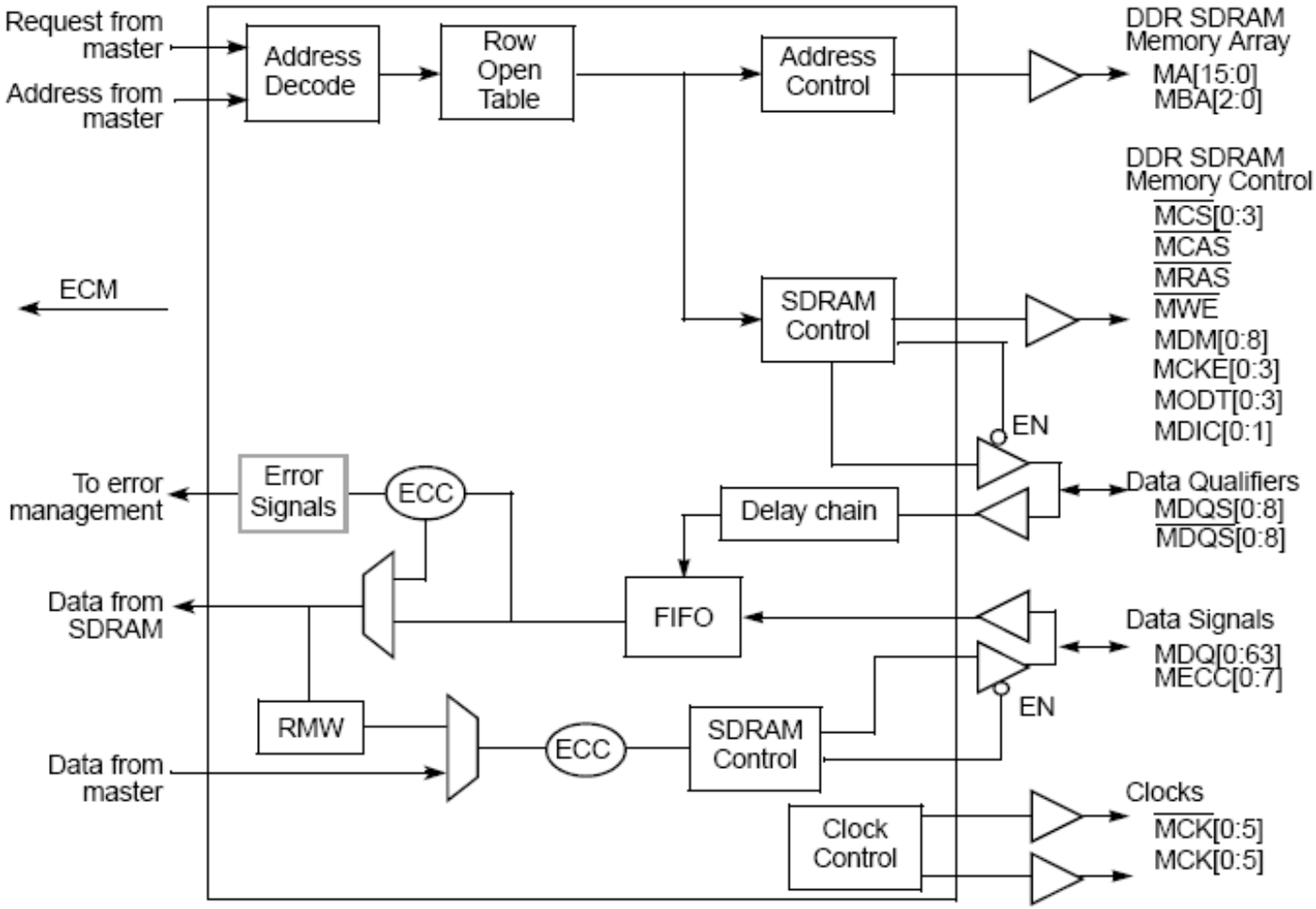
Typical Freescale DDR2/3 Controller Highlights

- Interface speed
  - DDR2 - up to 800 MHz
  - DDR3 - up to 800 MHz today (PowerQUICC® MPC8572, QorIQ™ P2020)
    - Evaluating higher speeds 1066 MHz and up to 1600 MHz
- Support Interface width
  - 64/72-bit data bus – high end product
  - 32/40-bit data bus – low end products
  - 16/24-bit data bus – low end products
- Discrete, unbuffered, and registered DIMM support
  - Memory device densities from 64 Mb – through 8 Gb
  - Up to four chip selects supported
  - Support for x8/x16 DDR devices – x4 devices are not supported
- Full ECC (Error Correction Code) support
  - Single error correction/detection, double error detection
  - Error injection for software development
- Self refresh support

Typical Freescale DDR2/3 Controller Highlights (cont'd)

- Read-Modify-Write support for Atomic Inc, Dec, Set, Clear, and sub-double word writes
- All timing parameters are under SW control
- Automatic data initialization (easy ECC support)
- Differential or single-ended data strobes
  - Differential option only available for DDR2 memories
  - DDR3 only implements differential DQS signals
- Dedicated open row table for each sub-bank
  - Up to 32 simultaneous open rows with 4 chip selects
- Up to six diff clock pairs
  - Eliminates the need for any external clock PLLs
- ODT support (both internally and externally), on-chip ZQ driver calibration
- SSTL-1.8, and SSTL-1.5 compatible IOs

Memory Controller Block Diagram



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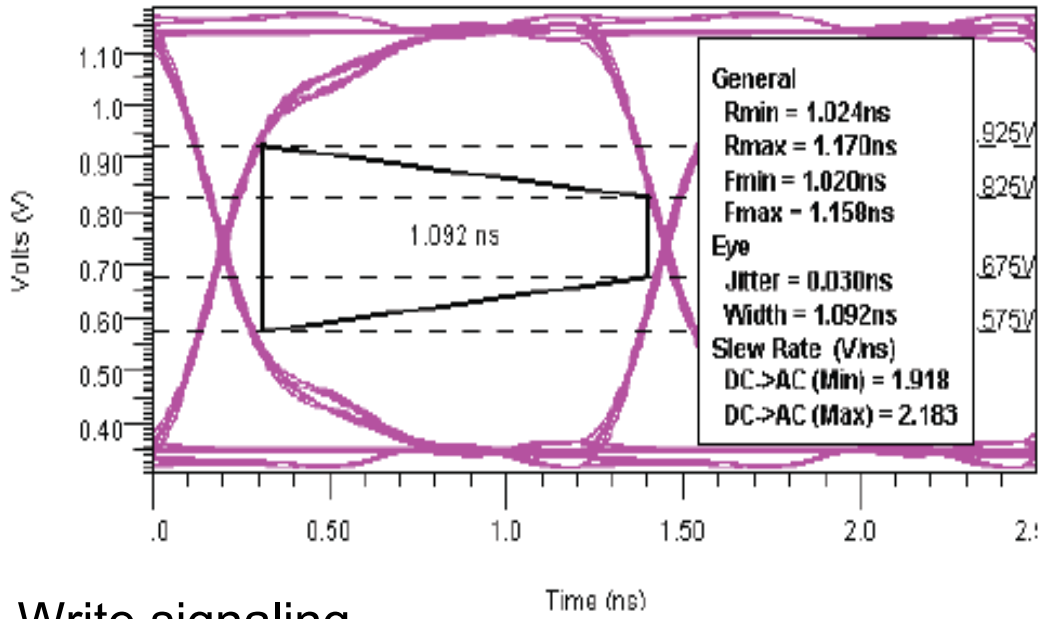
Key DDR3 Memory Improvements and Additions

- Lower signaling standard
- Reduced power
- Improved device pinout
- Fly-by architecture
- Write leveling
- Dynamic ODT for improved Write signaling
- Driver calibration
- Device reset
- DIMM address mirroring



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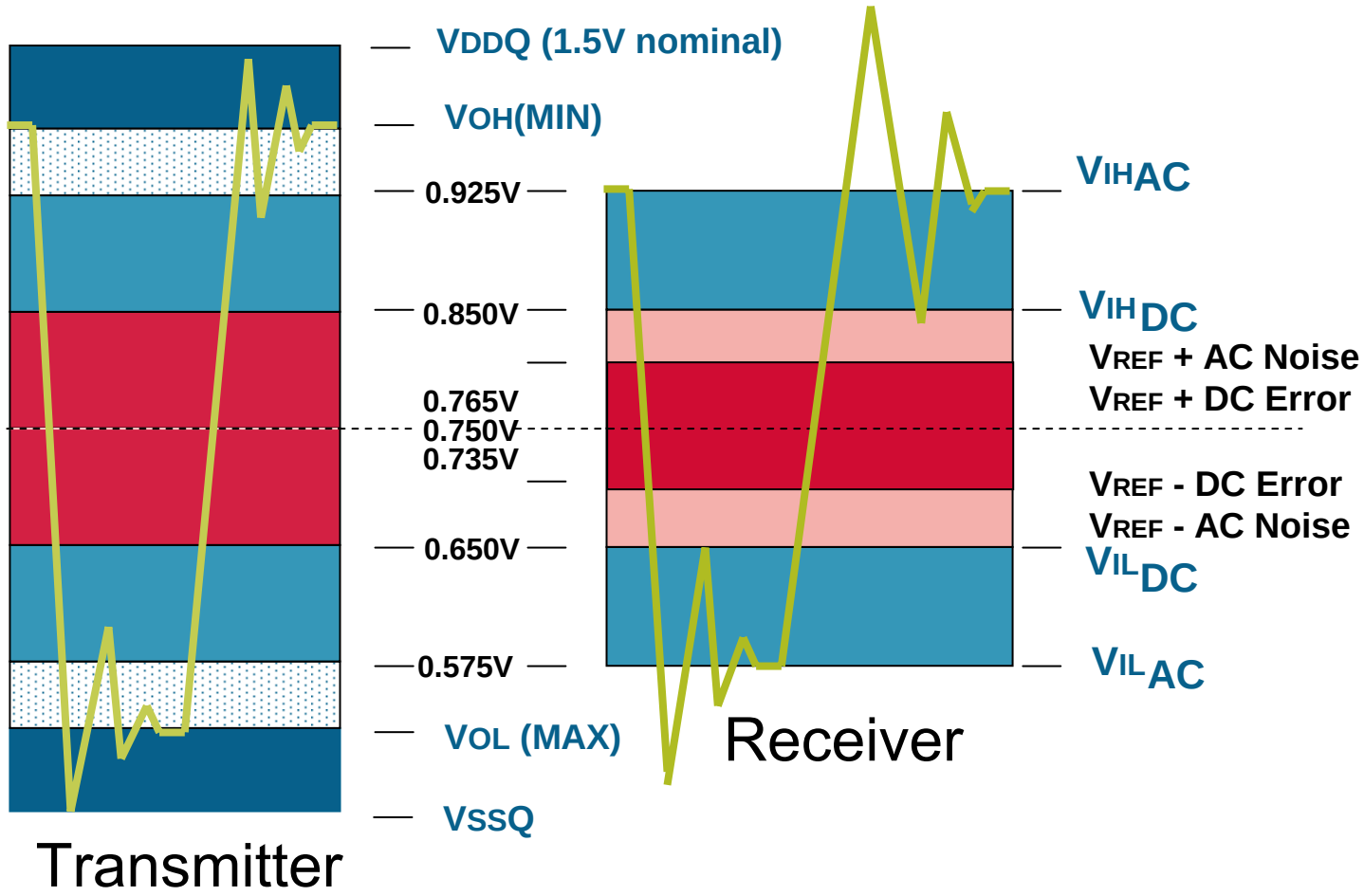
DDR3 Signaling – Example SSTL-1.5



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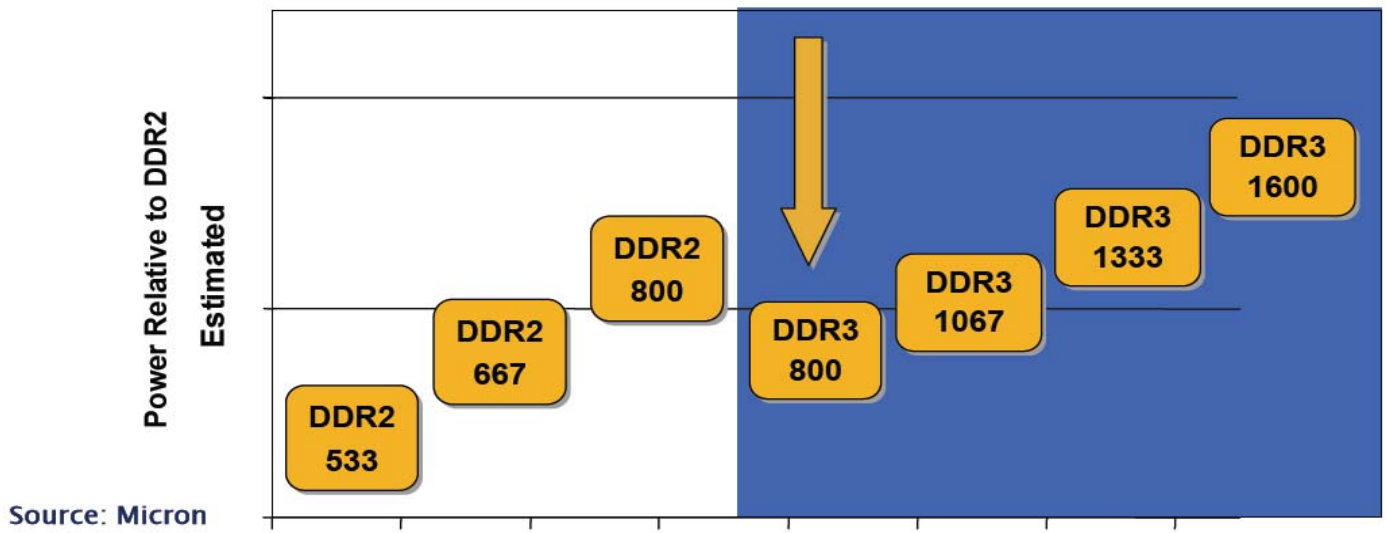
Lower Power

- Supply voltage reduced from 1.8V to 1.5V
  - ~ 30% power reduction (Micron claim)
  - ~ 25% is JEDEC's official claim
    - Compared to DDR2 at same frequency bin
- Lower I/O buffer power
  - 34 ohm driver vs. 18 ohm driver at memory device
- Improved bandwidth per Watt



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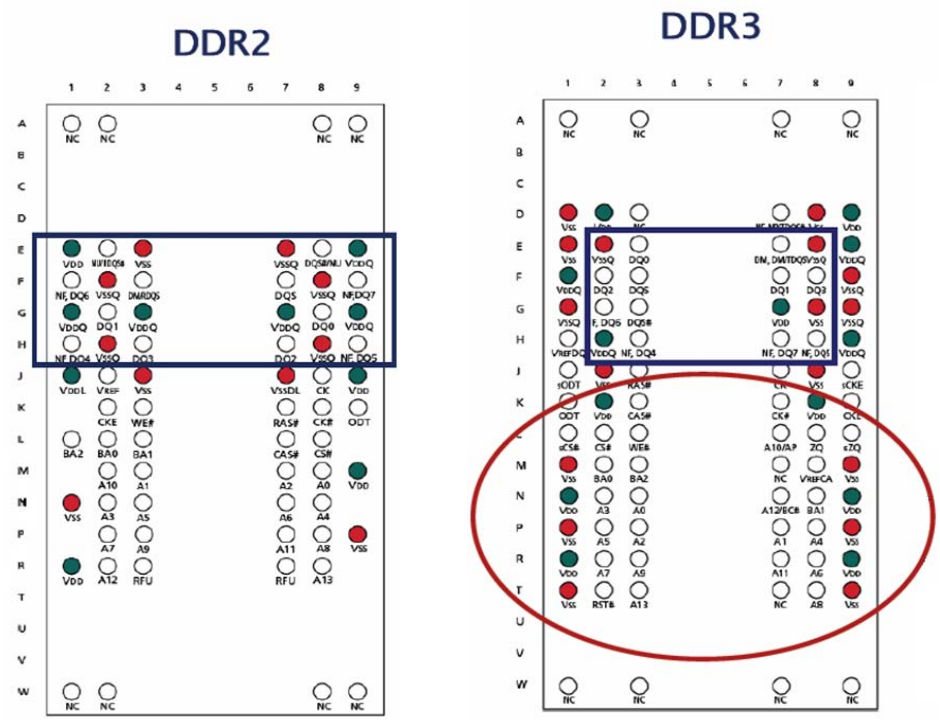
Improved Pinout

- Improved power delivery
  - More power and ground balls
- Improved signal quality
  - Better power and ground distribution
  - Better signal referencing
- Fully populated ball grid
  - Stronger reliability
- Improved pin placement
  - Less pin skew
  - Tighter timing leaving chip



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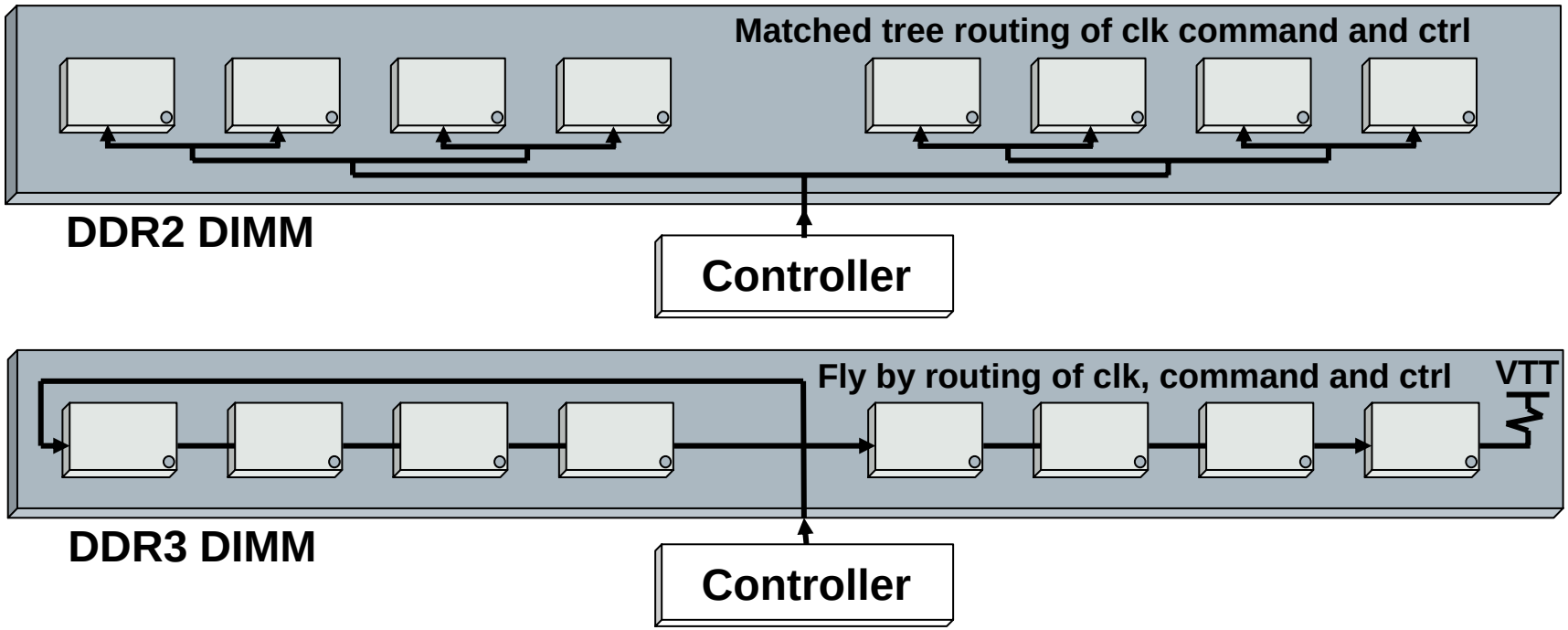
Fly-by Routing Topology

- Introduction of “Fly-by” architecture
  - Address, command, control and clocks
  - Improved signal integrity…enabling higher speeds
  - On module termination



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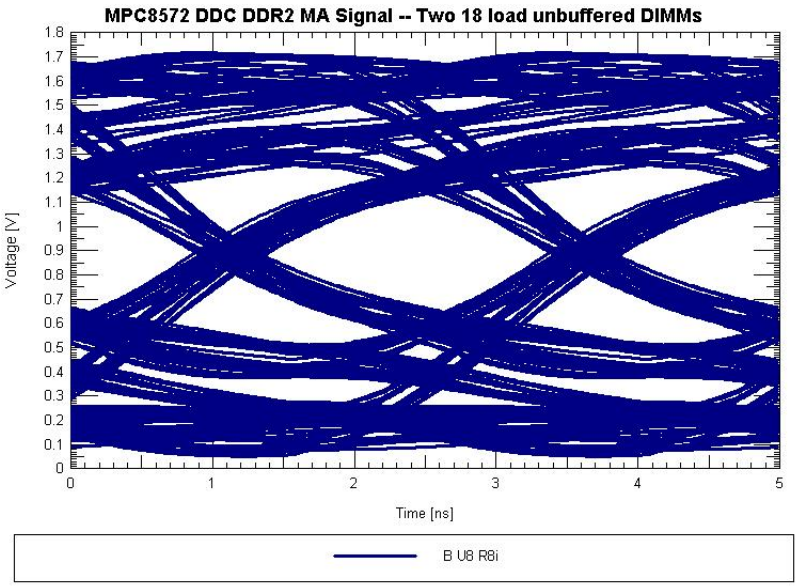
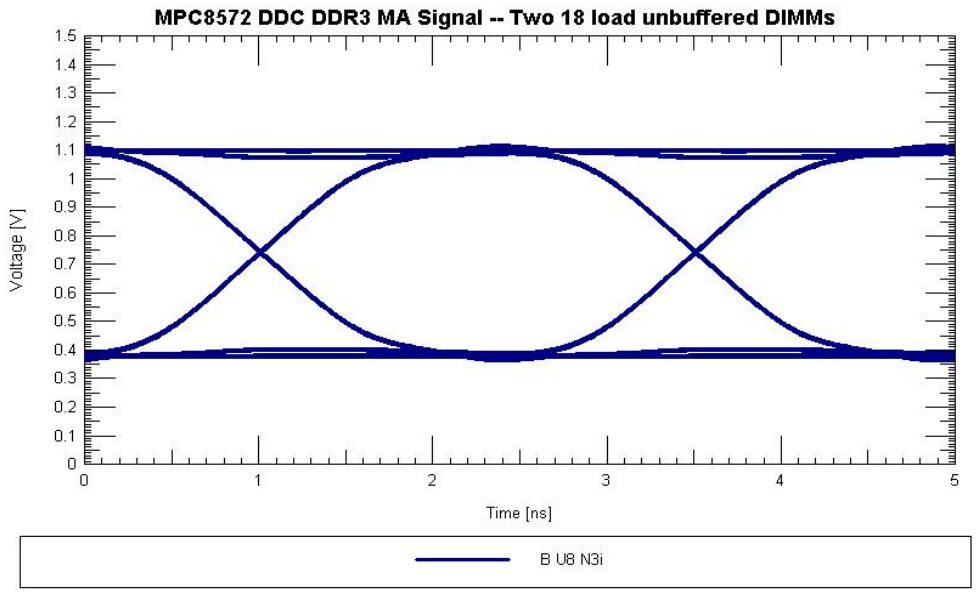
Fly-by Routing Improved SI

DDR2 Matched tree routing



DDR3 Fly-by routing



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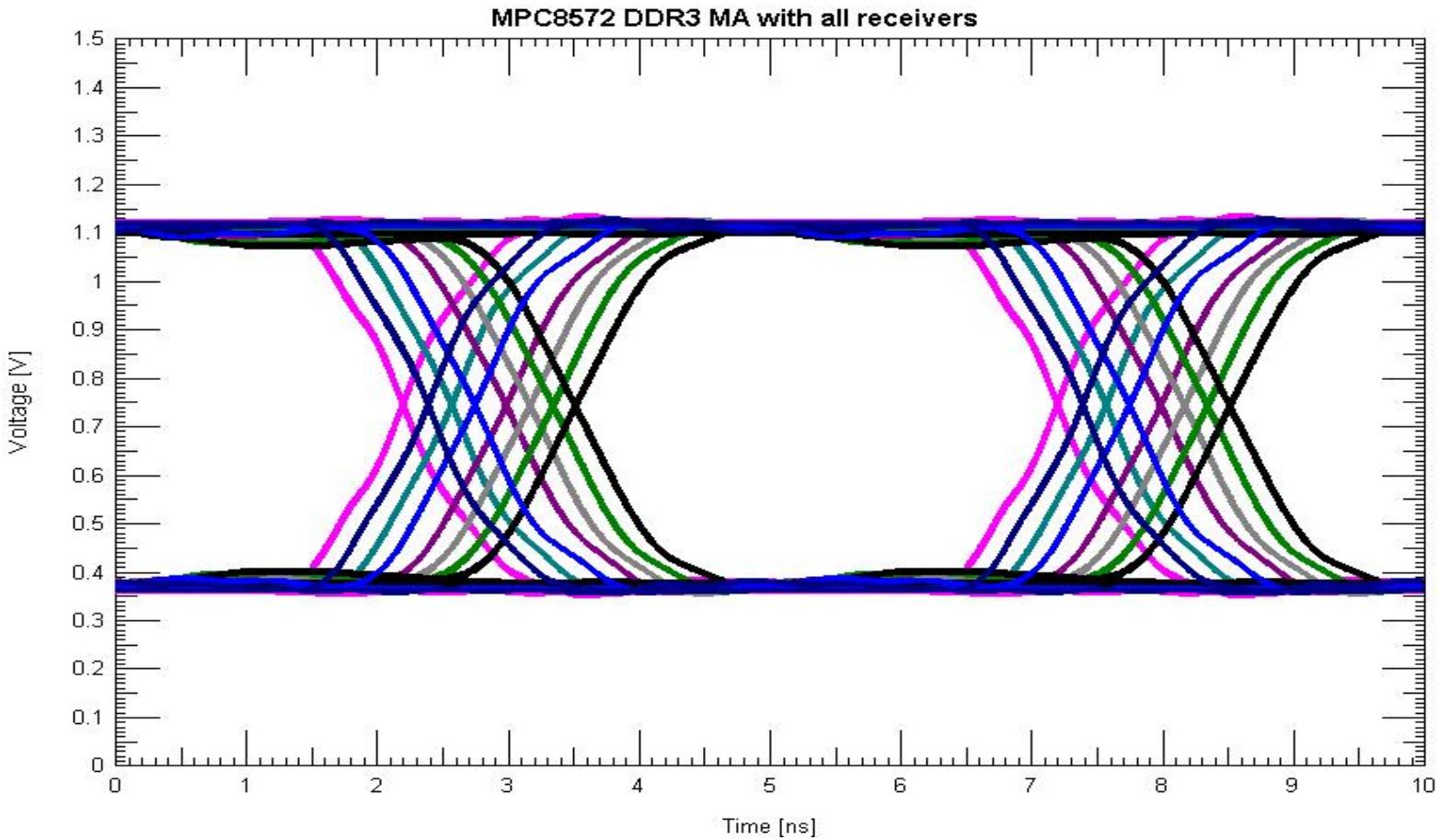
Fly-by Skew Across All Receivers



This illustrates the skew created by DDR3 fly-by routing

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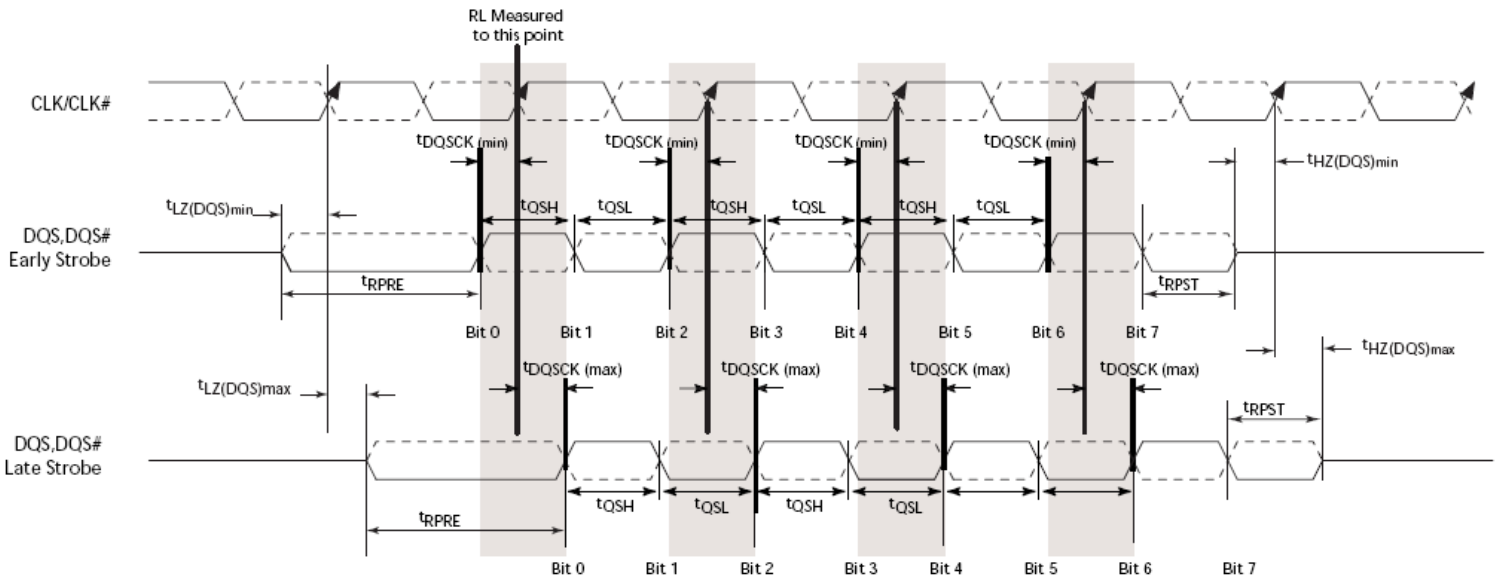
The Need for Write-Leveling….

- tDQSS requirement:
  - DQS/DQS# rising edge to CK/CK# rising edge
  - Clock to Strobe should be within a certain range for proper write operation to DDR3 SDRAMs

- tDQSS spec: +/- 0.25*tck



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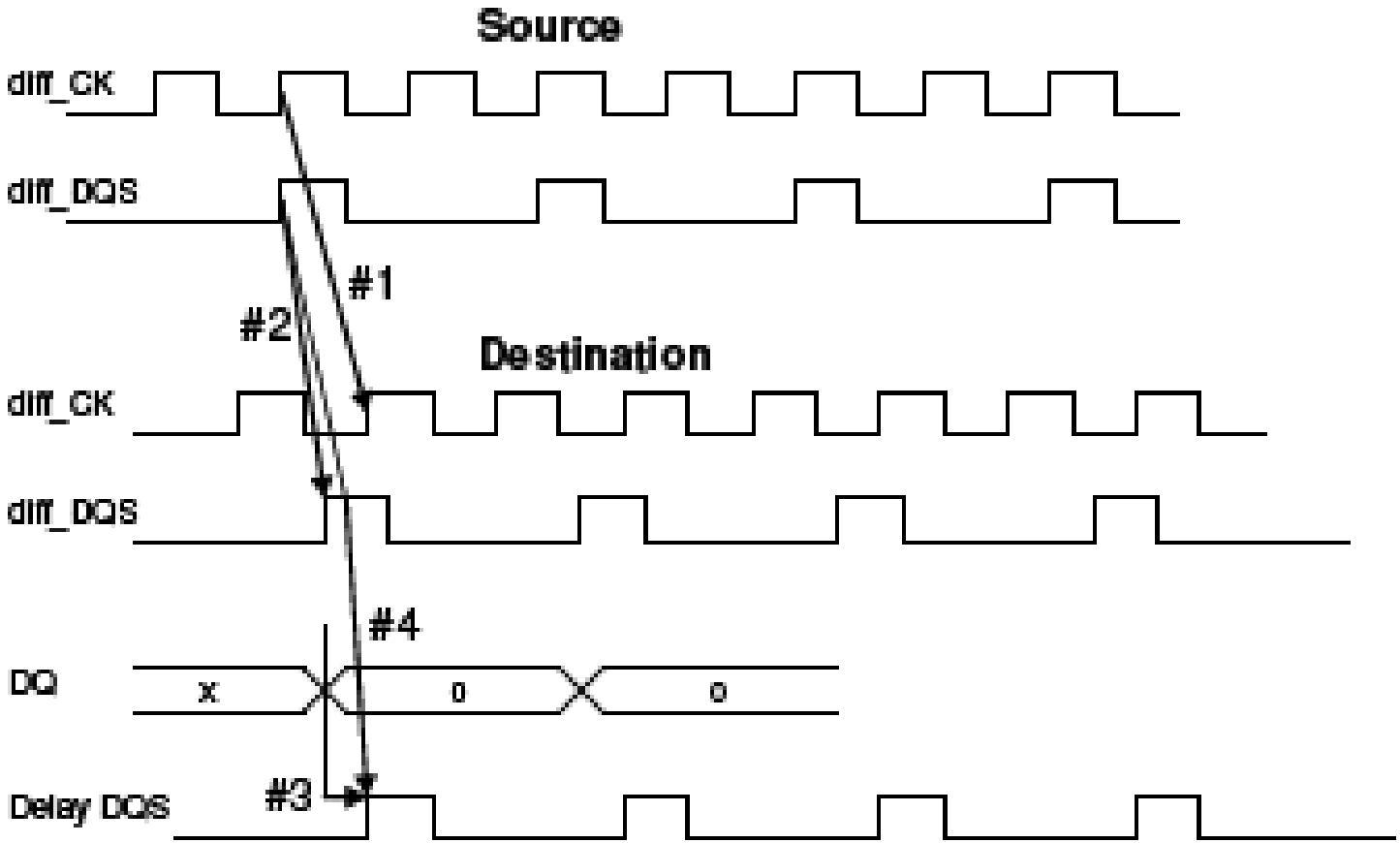
Write-Leveling… How it Works



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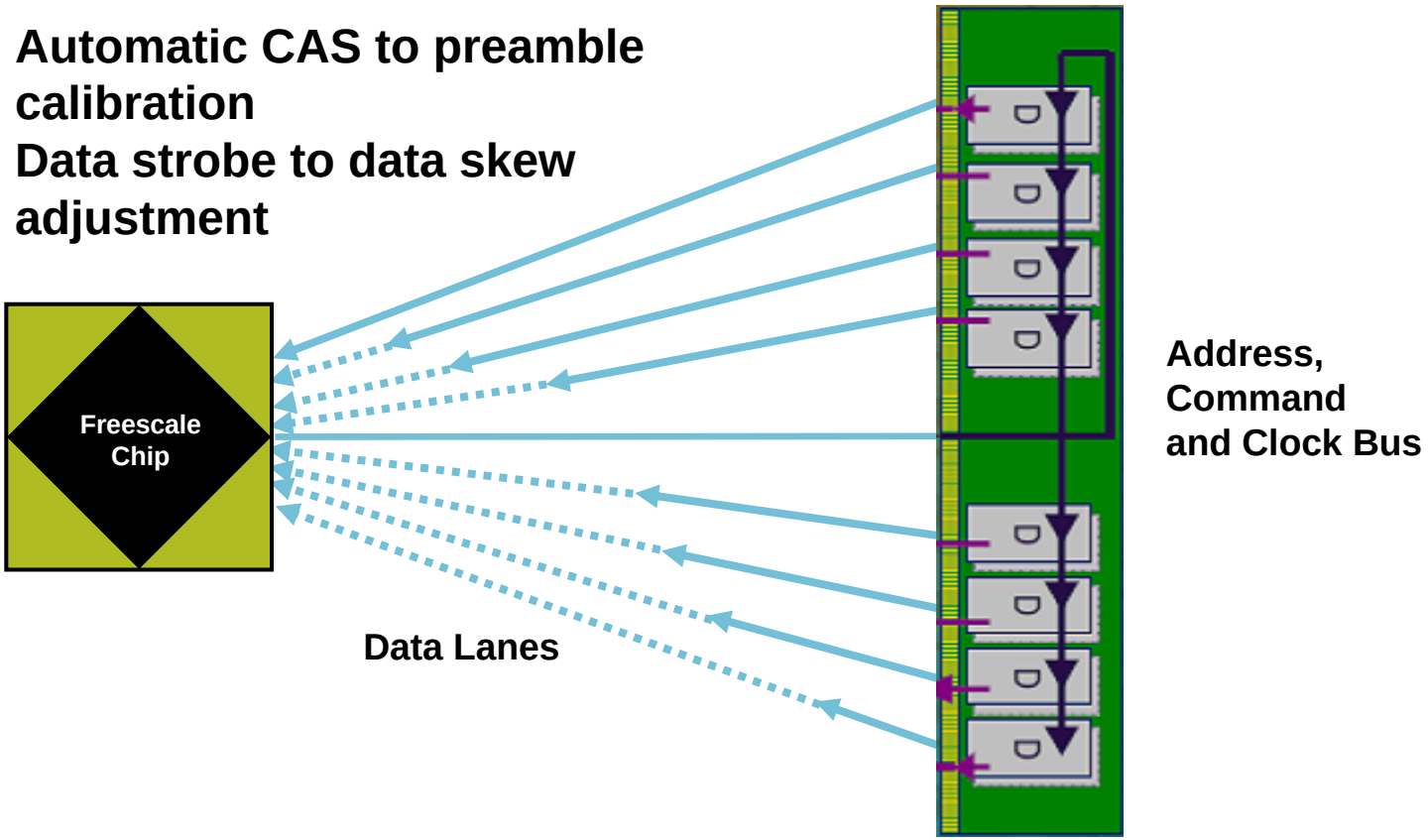
Read Adjustment

- Automatic CAS to preamble calibration
- Data strobe to data skew adjustment



Instead of JEDEC's MPR method, Freescale controllers use a proprietary method of read adjust method which will work with DDR2 and DDR3. This provides comparable performance to JEDEC's DDR3 MPR method

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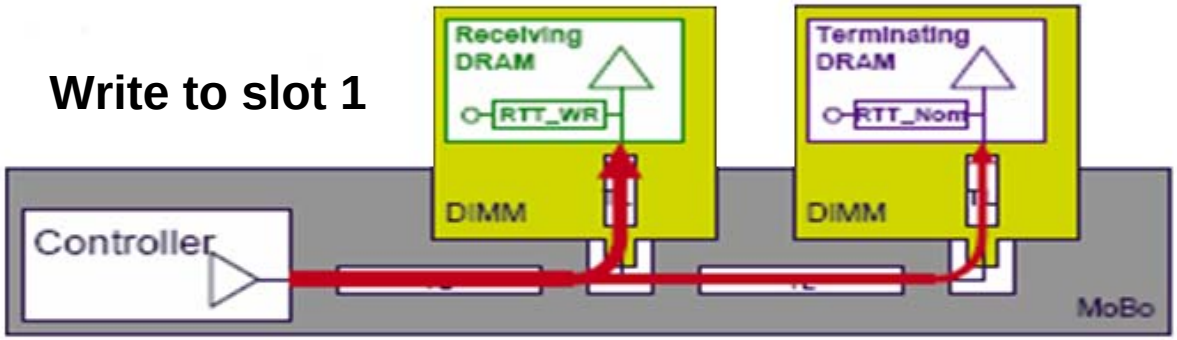
Dynamic ODT – System Motivation

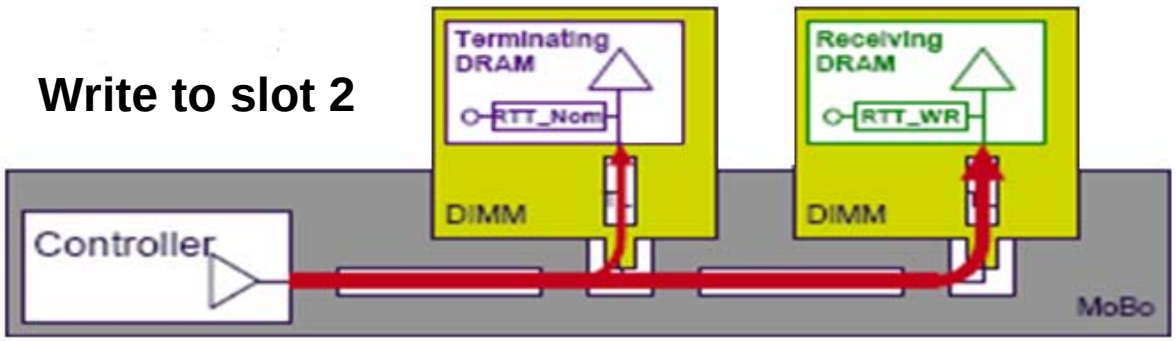
Example of termination scheme in application

Transaction	Slot 1	Slot 2
Write to Slot 1	RTT_WR = 120 Ω	RTT_Nom = 20 Ω
Write to Slot 2	RTT_Nom = 20 Ω	RTT_WR = 120 Ω

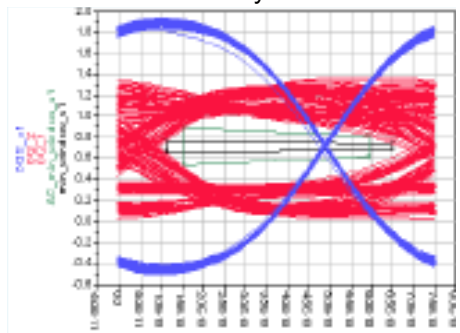
Write to slot 1



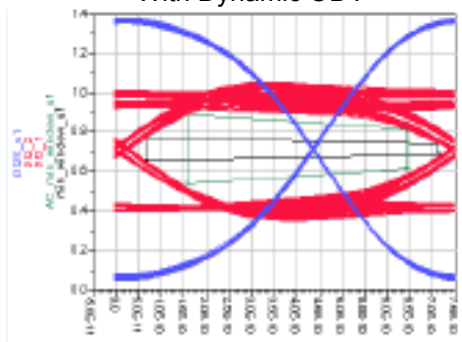
Write to slot 2



Without Dynamic ODT



With Dynamic ODT



Significant improvement of write signal integrity with DDR3 dynamic ODT

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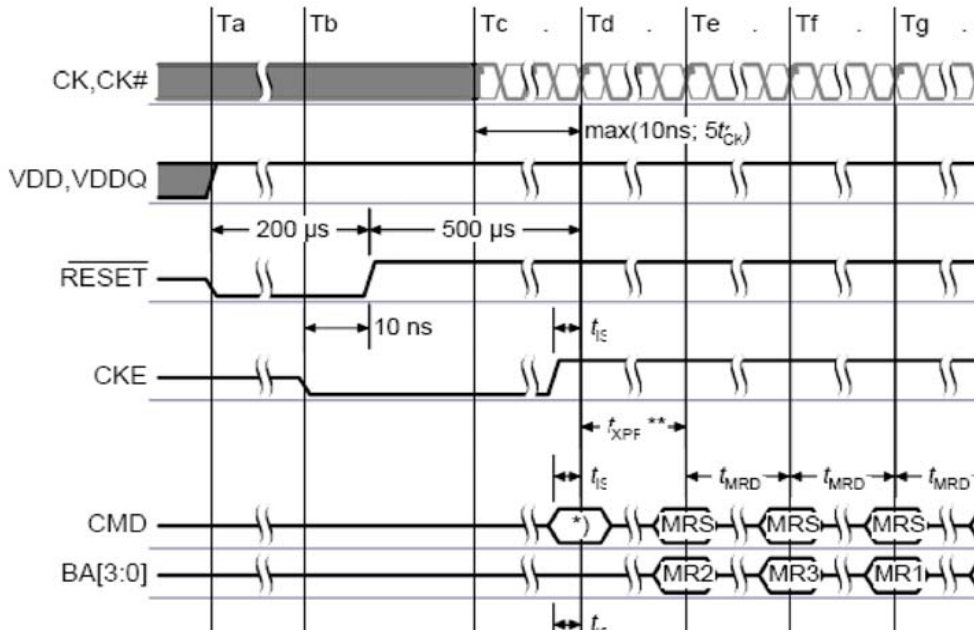
New DDR3 Pins

- Introduction of an asynchronous RESET# pin
  - Prevent Illegal commands and/or unwanted states
    - Cold reset
    - Warm reset
  - Known initialization
    - Resets all state information
    - No power-down required
    - Destructive to data contents



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New DDR3 Pins… cont'd

- VREF broken into separate banks (..at the DDR3 memories)
  - VREFCA
    - Used for the command / address signals
    - Decoupled to VDD plane
  - VREFDQ
    - Used for the data signals
    - Decoupled to VDD plane

- Key premise – noise reduction and coupling between the groups

At the DDR3 controller the same source driving VREFDQ to the memories would drive the controller VREF pin.

NEW DDR3 Pins – ZQ Calibration Pin

- The RZQ resistor is connected between the DDR3 memory and ground
  - Value = 240 Ohm +/- 1%
  - Permits driver and ODT calibration over process, voltage and temperatures
- Easier and more accepted than DDR2's (optional) OCD method
- Our controllers support both ZQ calibration commands
  - ZQCL – used during initialization (…takes longer)
  - ZQCS – used during normal operation (…periodic and takes less time)

Table 9-26. DDR_ZQ_CNTL Field Descriptions

Bits	Name	Description
0	ZQ_EN	ZQ Calibration Enable. This bit determines if ZQ calibrating will be used. This bit should only be set if DDR3 memory is used (DDR_SDRAM_CFG[SDRAM_TYPE] = 3'b111). 0 ZQ Calibration will not be used. 1 ZQ Calibration will be used. A ZQCL command will be issued by the DDR controller after POR and anytime the DDR controller is exiting self refresh. A ZQCS command will be issued every 32 refresh sequences to account for VT variations.

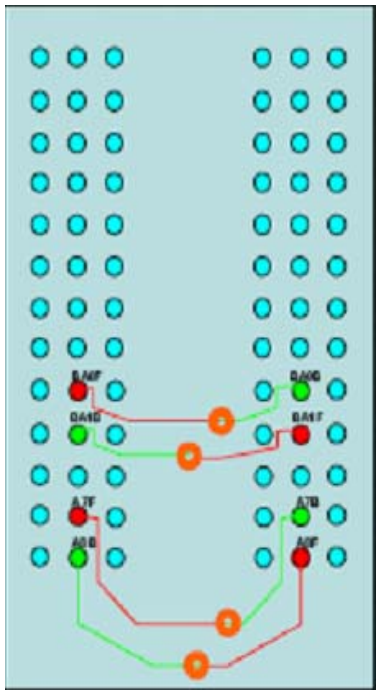
Freescale Controller Driver Calibration

- Our Freescale controller also does driver calibration
  - Enabled by software
  - Occurs automatically during initialization after MEM_EN is set

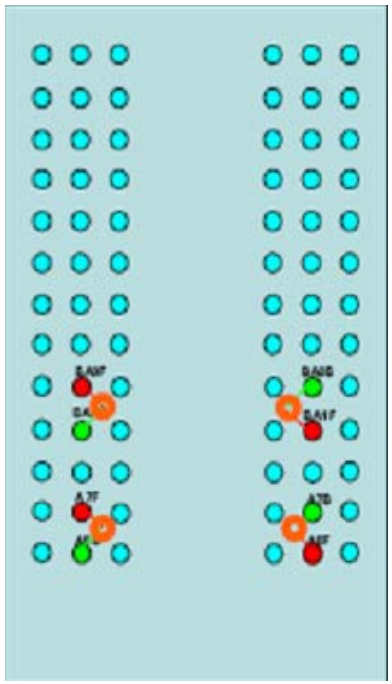
- MDIC precision resistors are used at our controller
  - Value = 40 Ohms 1% tolerance

DIMM Mirroring…

- The DDR3 IP fully supports address mirroring



Non-Mirrored



Mirrored

Edge Connector Signal	SDRAM Pin, Standard	SDRAM Pin, Mirrored
A0	A0	A0
A1	A1	A1
A2	A2	A2
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
A9	A9	A9
…	…	…
A15	A15	A15
BA0	BA0	BA1
BA1	BA1	BA0
BA2	BA2	BA2

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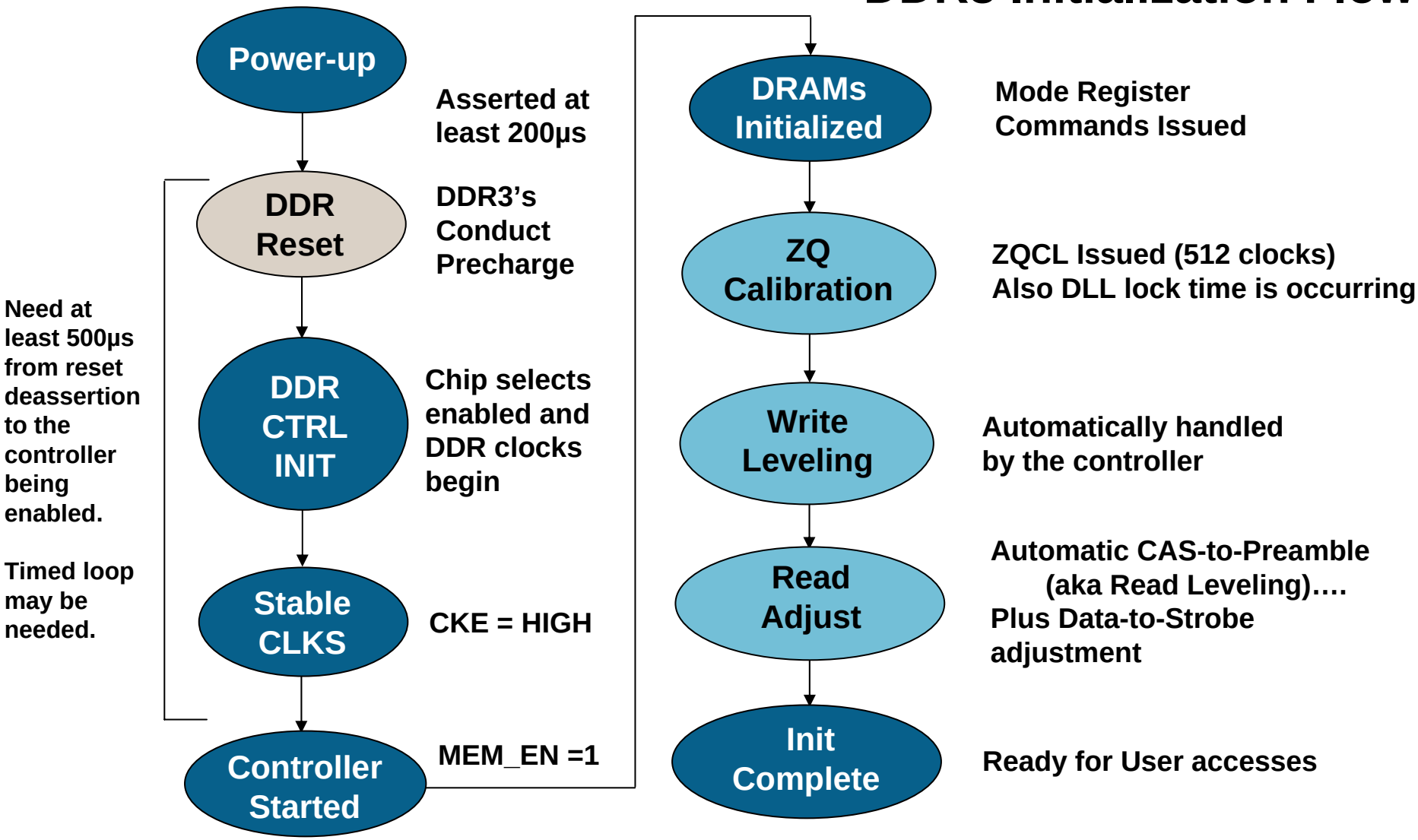
NEW DDR3 Pins – TDQS/TDQS#

- TDQS/TDQS# New pin on x8 DDR3 devices
  - Not present on x4 or x16 devices
  - Allows combinations of x4/x8 devices in the same system

- We don’t support TDQS/TDQS#
  - We do not support x4 devices… so this function is not supported

DDR3 Initialization Flow



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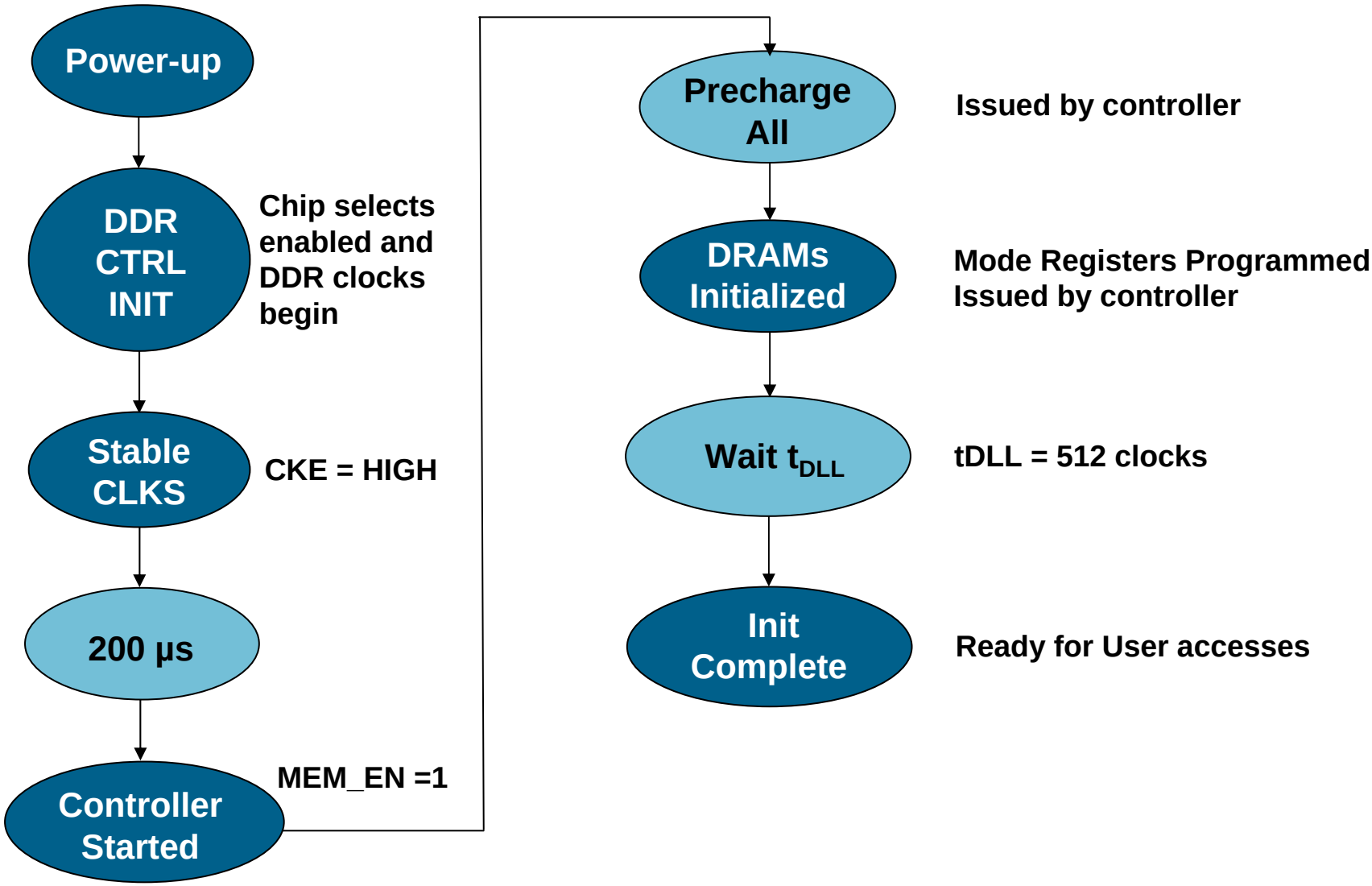
DDR2 Initialization Flow



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Power-up: Power Rails

- DDR3 memories have two power pins defined
  - Same voltage level of 1.5V nominal
  - Separate pins help reduce power supply noise/interruption
  - VDD – Core Power
  - VDDQ – IO Power

- Therefore, there will be 2 different cases:
  - Case 1 – two separate sources
  - Case 2 – single voltage source for both rails

Power-up: Power Rails cont'd

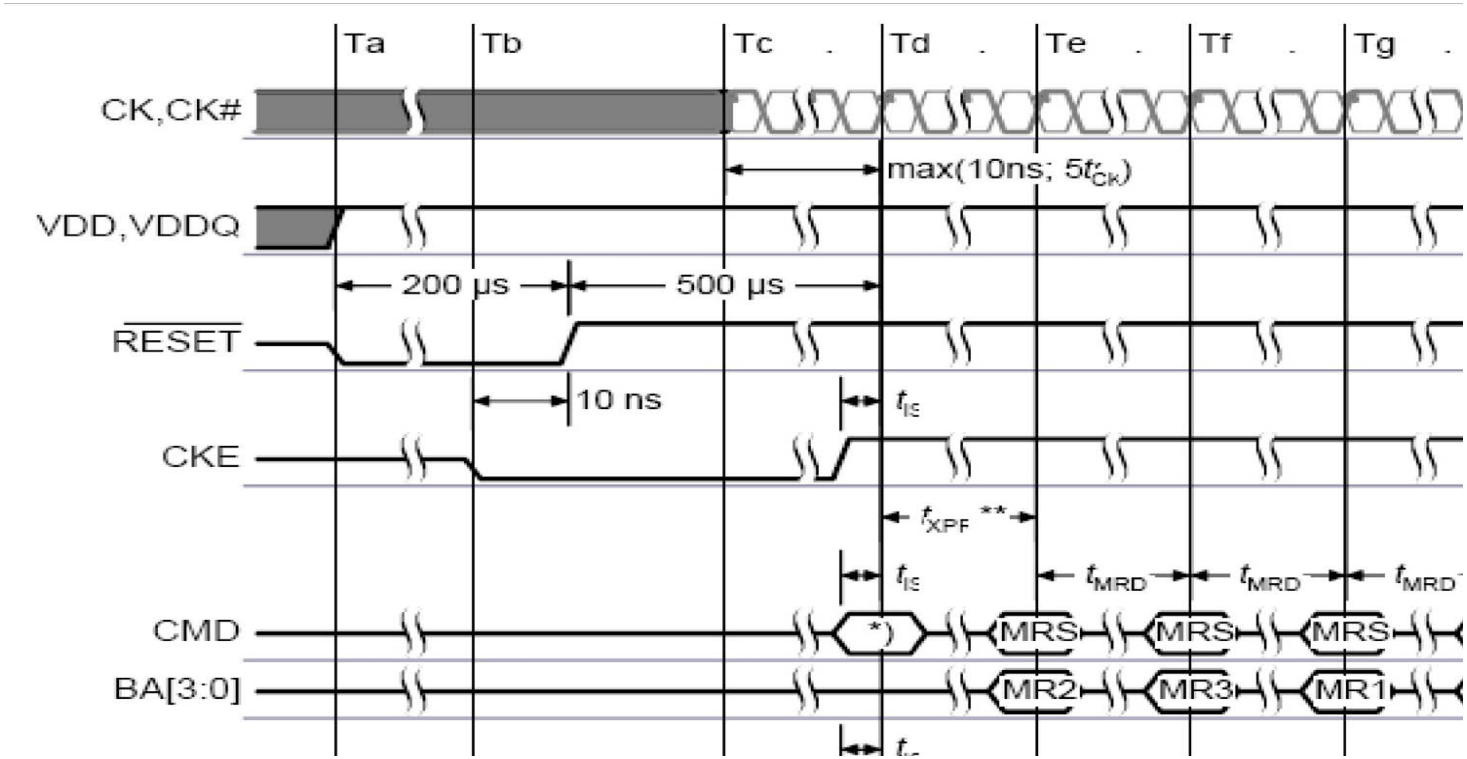
- The following should be applied whether a single voltage source or separate voltage sources are used:
  - Apply Power
    - RESET# is recommended to be maintained below 0.2V X VDD (min 200 µs) and all other inputs may be undefined
  - The voltage ramp time between 300mV to VDDmin must be no greater than 200 ms
    - VDD > VDDQ, VDD-VDDQ < 0.3V
  - The voltage levels on all other pins should not exceed VDD/VDDQ or be below VSS/VSSQ

Reset

- Starting with DDR3, a reset function is supported
  - All devices have a dedicated RESET# pin, operating at CMOS levels
  - Low pass filter incorporated – prevents accidental glitches
  - Voltage level of the pin should be carefully maintained to prevent loss of data
- Reset should be done after the power supply voltage level(s) are properly up and stabilized
- Reset can also be issued whenever “Warm-booting” is needed
- Destructive to data contents, therefore memories will need to be re-initialized

Stable Clocks

- Clocks are started as soon as a chip select is enabled
  - Controller will ensure that the appropriate clock to CKE relationship is met



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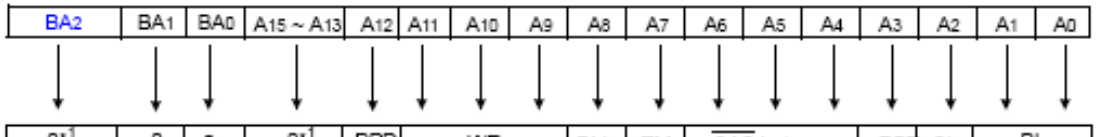
DRAMs Initialized

- Once clocks are stabilized, the next step should be to set the Mode Register
  - Mode Registers set the operational mode of the DDR3 DRAMs
  - Order of programming:
    - MR2 > MR3 > MR1 > MR0

- Several new features for DDR3, such as:
  - MR0 : Burst length control (BC4/8 on the fly)
  - MR1 : Write-leveling enable
  - MR2 : RTT_WR, CWL, ASR

Mode Register Set 0



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

Item#1586.05/06(Mar.'05)

A1	A0	BL
0	0	8 (Fixed)
0	1	4 or 8(on the fly)
1	0	4 (Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	Reserved

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11(Optional for DDR3-1600)

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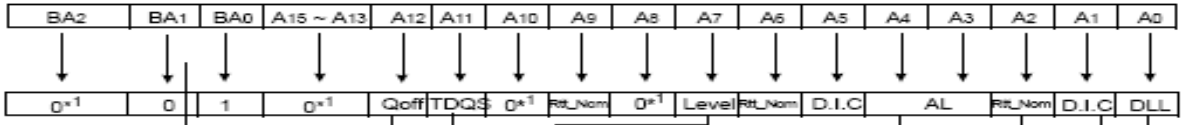
Mode Register Set 1



A11	TDQS enable
0	Disabled
1	Enabled

A7	Write leveling enable
0	Disabled
1	Enabled

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled *2

*2: Outputs disabled - DQs, DQSs, $\overline{DQS}$s.

A9	A6	A2	Rtt_Nom*3
0	0	0	ODT disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*2
1	0	1	RZQ/8*2
1	1	0	Reserved
1	1	1	Reserved

Note 1: RZQ = 240 Ω

Note 2: If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

Note 3: In Write leveling Mode (MR1 [bit7] = 1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

A0	DLL Enable
0	Enable
1	Disable

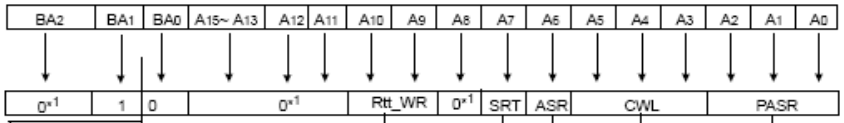
A5	A1	Output Driver Impedance Control
0	0	Reserved for RZQ/6
0	1	RZQ/7
1	0	RZQ/TBD
1	1	RZQ/TBD

Note 1: RZQ = 240 Ω

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Mode Register Set 2

MR2 Programming



A7	Self-Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended (optional) operating temperature range

A6	Auto Self-Refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable (Optional)

A10	A9	Rtt_WR
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A2	A1	A0	Partial Array Self-Refresh (Optional)
0	0	0	Full Array
0	0	1	HalfArray (BA[2:0]=000,001,010, &011)
0	1	0	Quarter Array (BA[2:0]=000, & 001)
0	1	1	1/8th Array (BA[2:0] = 000)
1	0	0	3/4 Array (BA[2:0] = 010,011,100,101,110, & 111)
1	0	1	HalfArray (BA[2:0] = 100, 101, 110, &111)
1	1	0	Quarter Array (BA[2:0]=110, &111)
1	1	1	1/8th Array (BA[2:0]=111)

I

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK ≥2.5ns)
0	0	1	6 (2.5ns >tCK≥1.875ns)
0	1	0	7 (1.875ns>tCK≥1.5ns)
0	1	1	8 (1.5ns>tCK≥1.25ns)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

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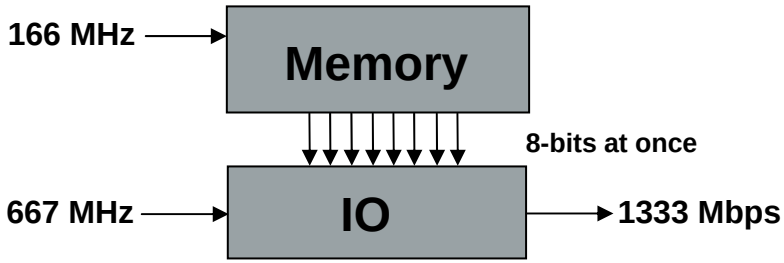
Driver Calibration

- DDR3 SDRAMs require a ZQ resistor (240 ohm +/- 1%) external to the device
  - Used as a reference for driver and ODT calibration
  - Allows both to remain stable – independent of thermal variation during operation

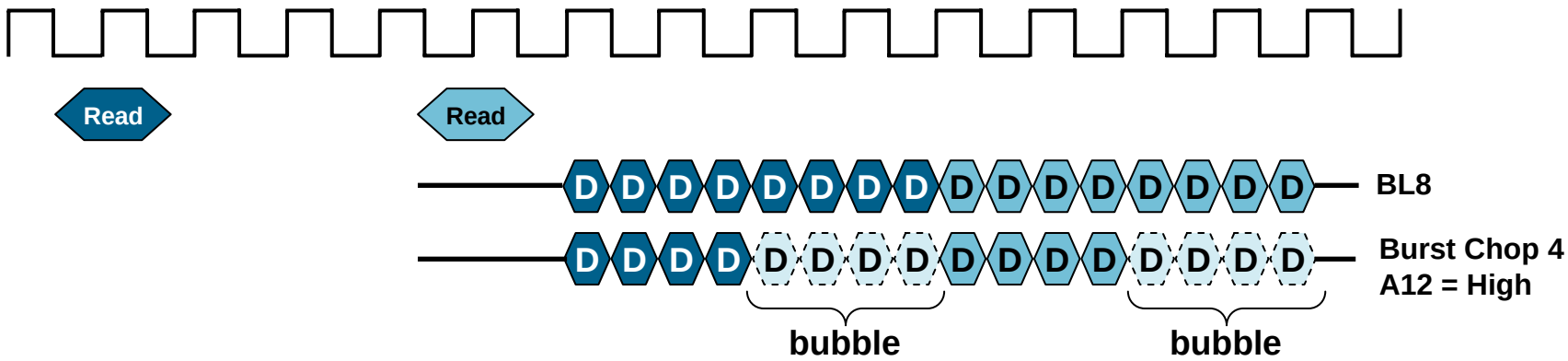
- Therefore, the last step in the initialization process is ZQ_long calibration sequence – after which the DDR3 memories are now ready for normal operation

Burst Length

- Burst Length control (BC4/8 on the fly)
  - 8-bit pre-fetch is standard for DDR3 memories
  - Thus, burst length of 8 is default



- DDR3's also support 'pseudo BL4' using burst chip



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Pitfall 1 – Noisy V_{REF}

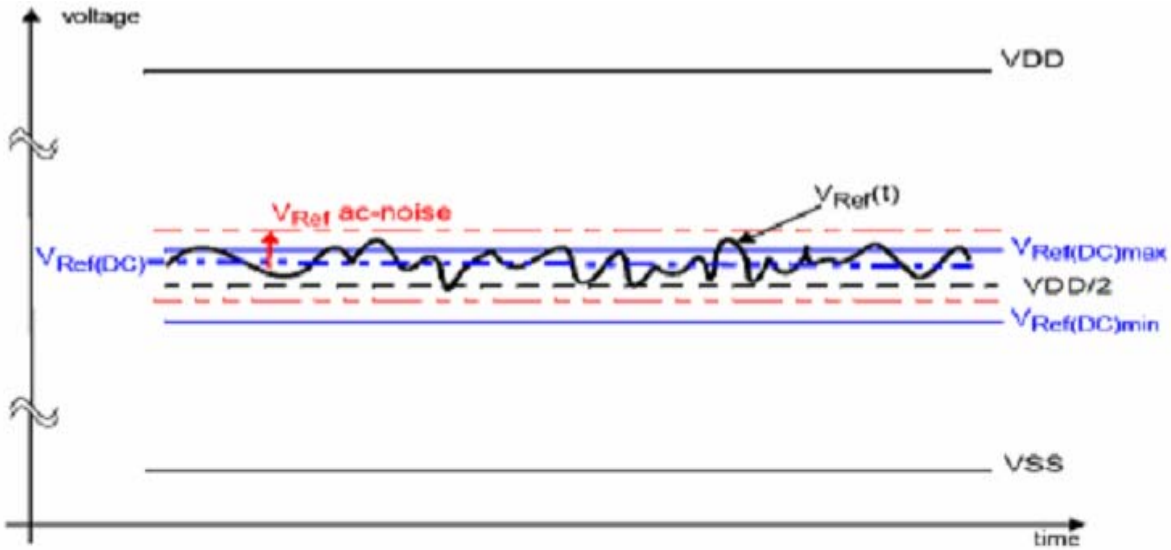

Figure 80 — Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

- VRef(t) may temporarily deviate from VRef(DC) by no more than +/- 1% VDD
- VRef(DC) is the linear average of VRef(t) over a very long period of time (e.g. 1 sec)

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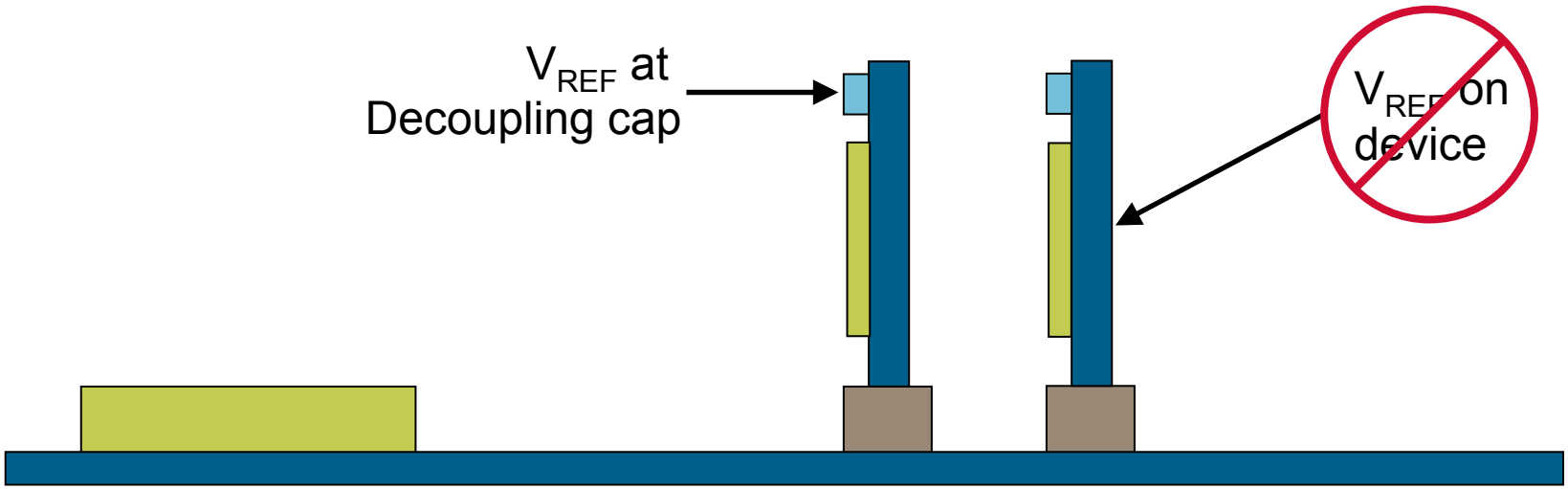
Pitfall 1 – Measuring V_{REF}

- **Measuring at device will likely give greater than 50 mV peak-to-peak**
  - Result of coupled noise from DDR device
- **V_{REF} system noise should be measured at capacitor nearest the memory device**



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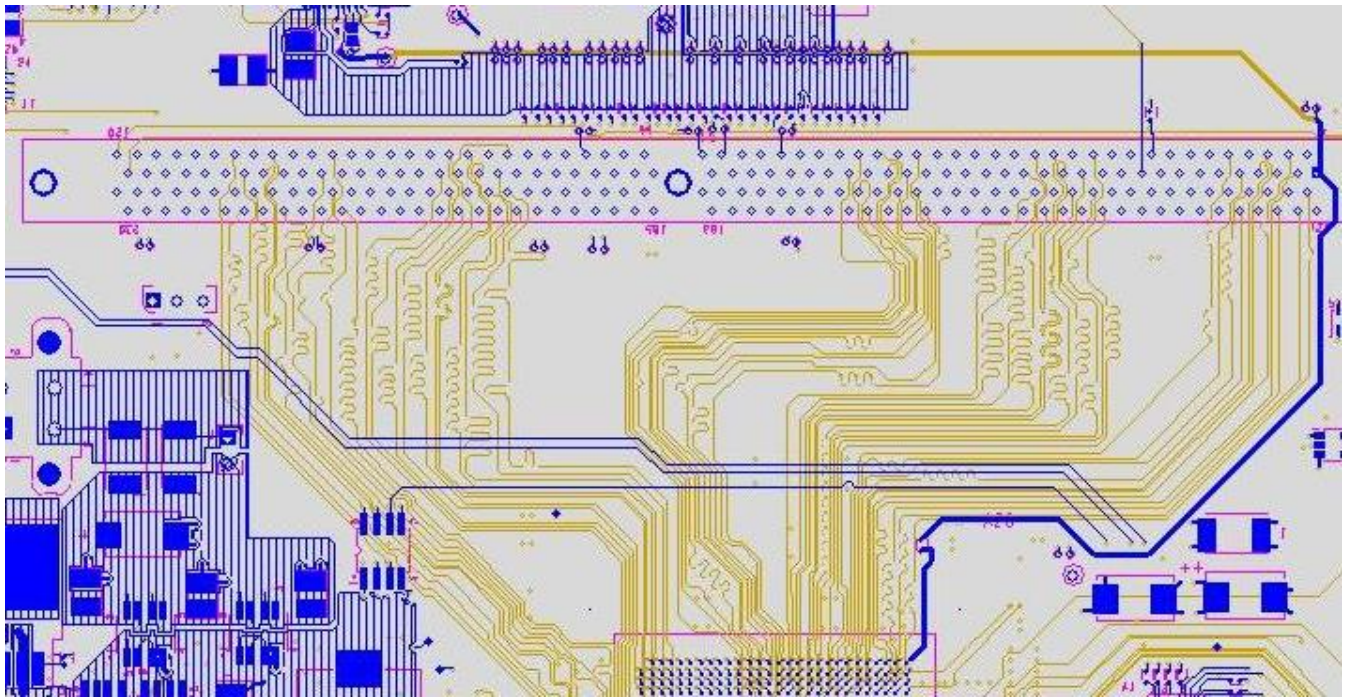
Pitfall 1 – Protecting V_{REF}

V_{REF}		
18.	Has V_{REF} been routed with a wide trace? (Minimum of 20–25 mil recommended.)	
19.	Has V_{REF} been isolated from noisy aggressors? In addition, maintain at least a 20–25 mil clearance from V_{REF} to other traces. If possible, isolate V_{REF} with adjacent ground traces.	
20.	Has V_{REF} been proper decoupled? Specifically, decouple the source and each destination pin with 0.1uf caps.	



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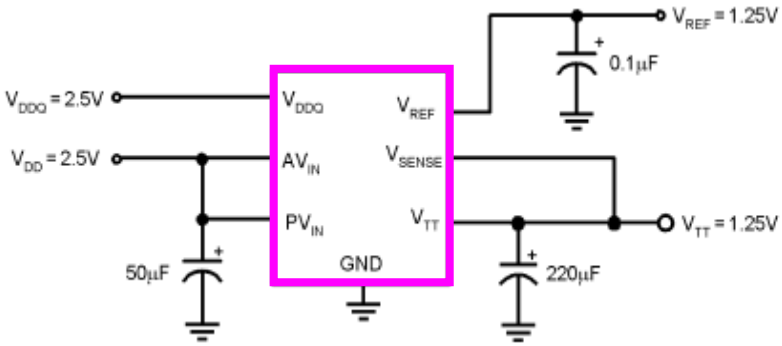
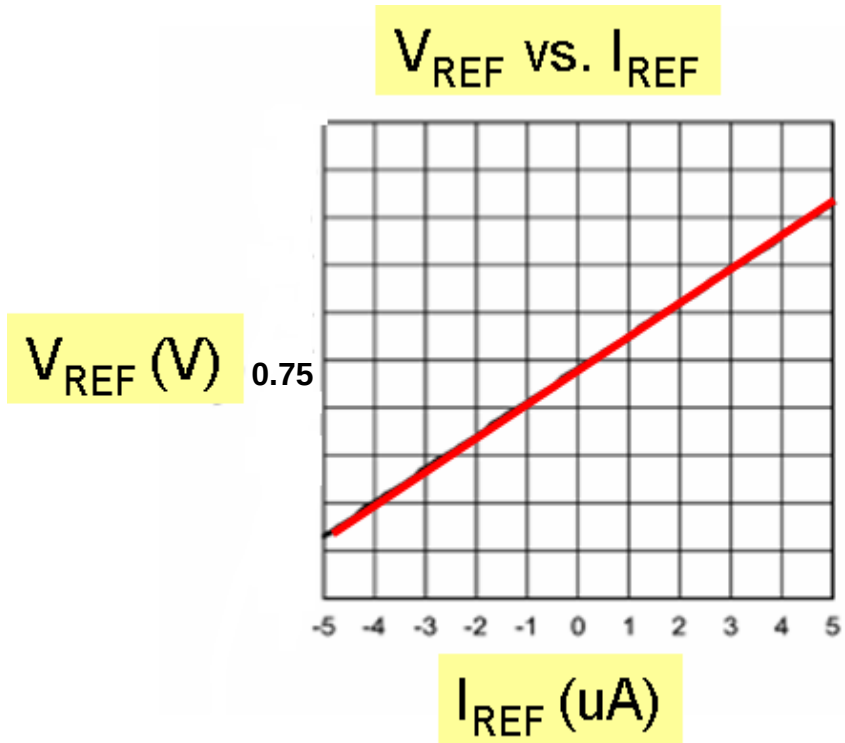
Pitfall 2 – Wimpy V_{REF} Source

- V_{REF} current consumption is typically 1.5-2.0 mA
- For most DDR regulators…. this is easily handled





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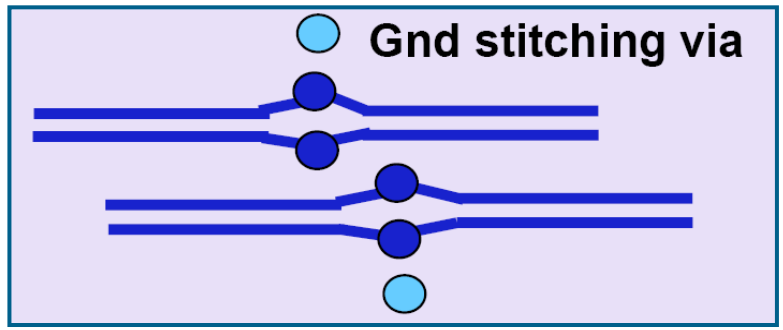
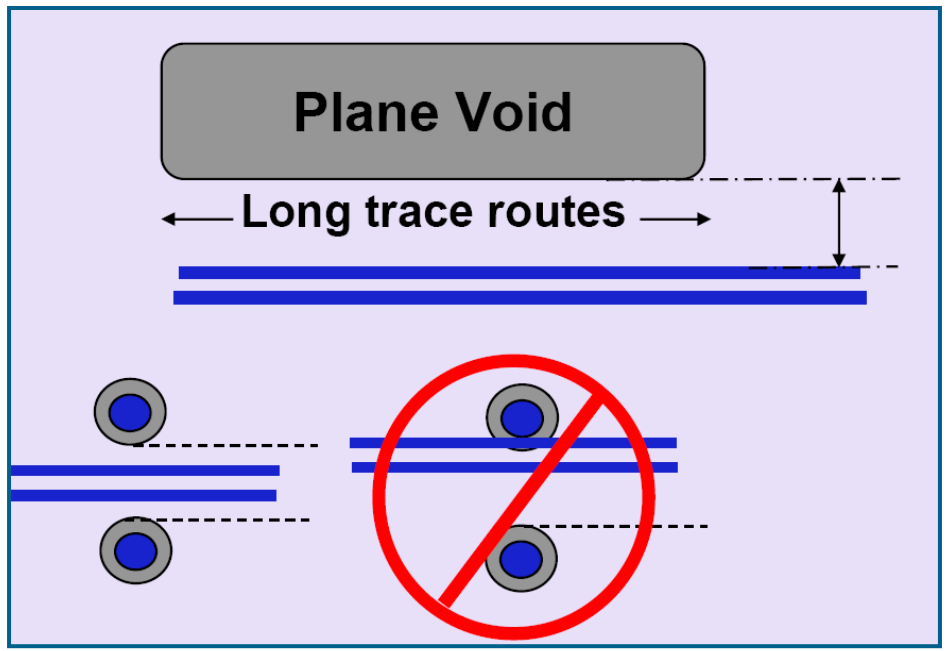
Pitfall 3 – Reference Plane Discontinuities

- **Contiguous reference plane**
  - GND – Data
  - Pwr - Address / Cmd
- **Use stitching vias if switching layers**



- **Keep away from plane voids**
- **Avoid crossing plane splits**
- **Avoid trace over anti-pad**



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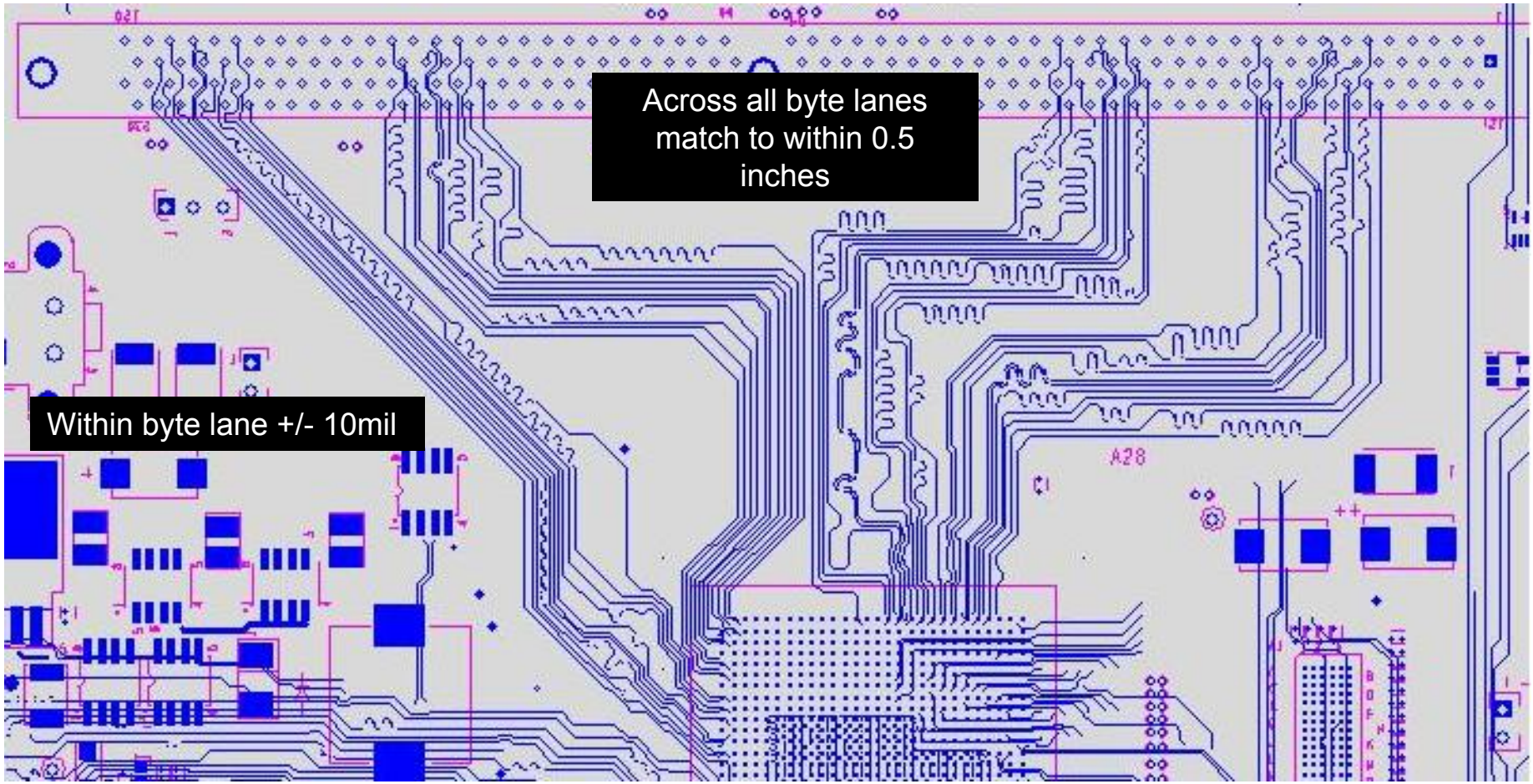
Pitfall 4 – Data Tuning



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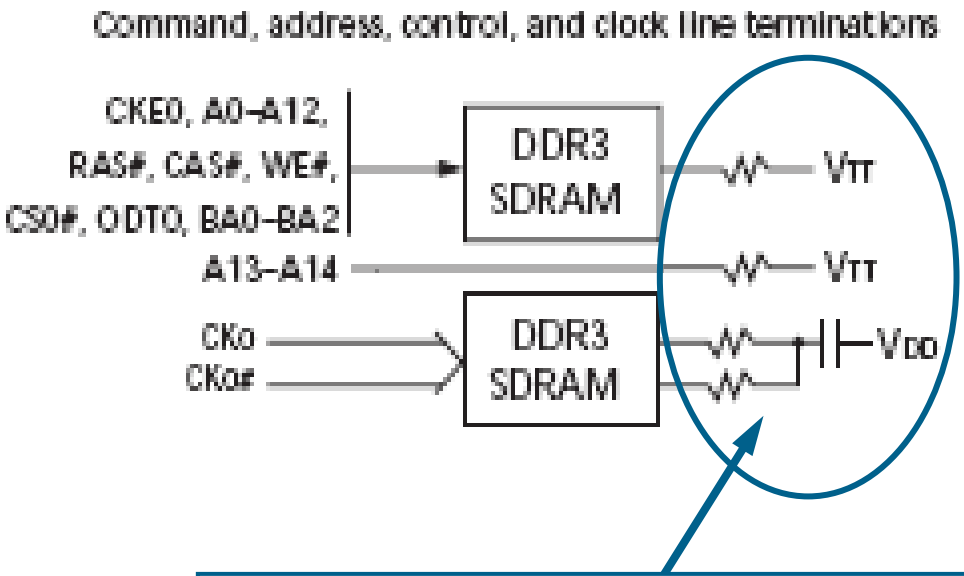
Pitfall 5 – Forgetting Termination



Still needed for soldered-down implementations.

DIMM modules have the termination on the module.

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Pitfall 6 – POR Config Selection

Table 4-18. DDR DRAM Type

Functional Signal	Reset Configuration Name	Value (Binary)	Meaning
TSEC2_TXD[1] Default (1)	cfg_dram_type	0	DDR2 1.8V, CKE low at reset
		1	DDR3 1.5V, CKE low at reset (default)

Above example assumes MPC8572. Other devices may utilize a different functional pin for the POR setting

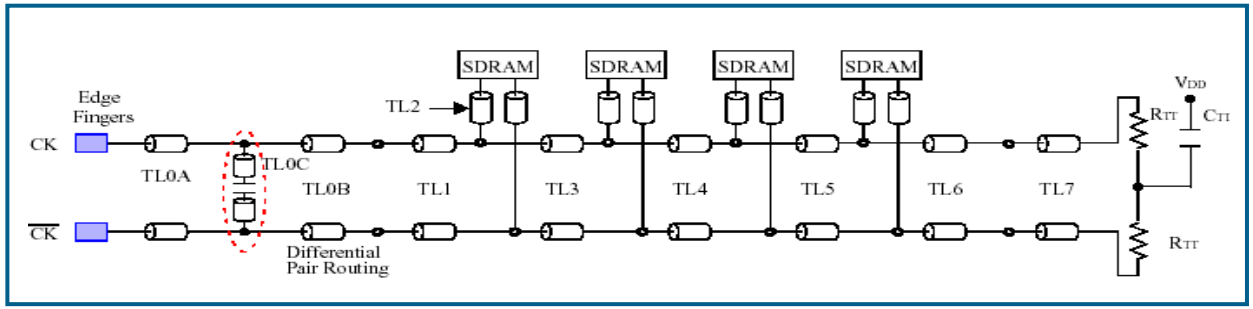
Pitfall 7 – Expandability

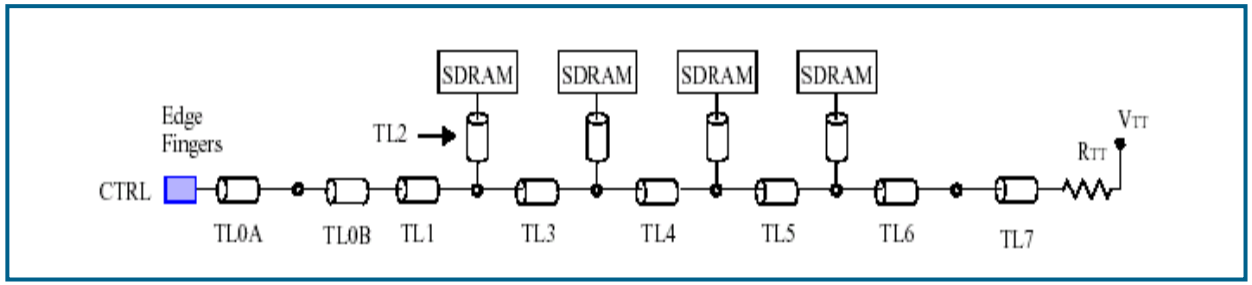
Signal Name	Pin Nomenclature	Signal Type	Function
A13	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on x4/x8 512 Mb and 1 Gb devices and all configurations of the 2 Gb or 4Gb.
A14	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on x4/x8 2 Gb devices and all 4 Gb configurations.
A15	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on 4 Gb (x4/x8).
BA2	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on all configurations of the 1 Gb, 2 Gb, and 4 Gb.

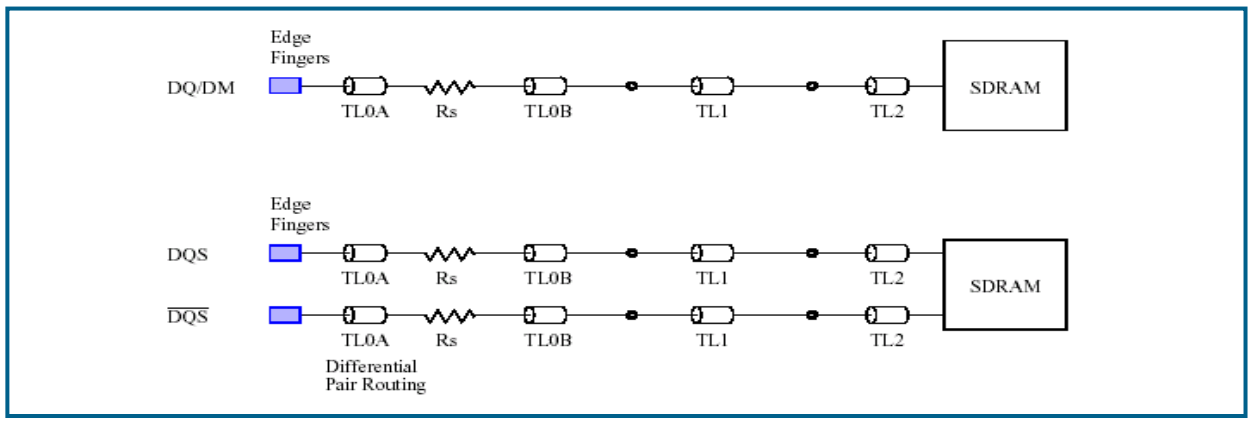
Rule of thumb:

For DDR3 - Every address (A0-A15), and all three bank address (BA0-BA2) line from our controllers should be connected to the memory subsystem.

Pitfall 8 – Not Using Proven JEDEC Topologies







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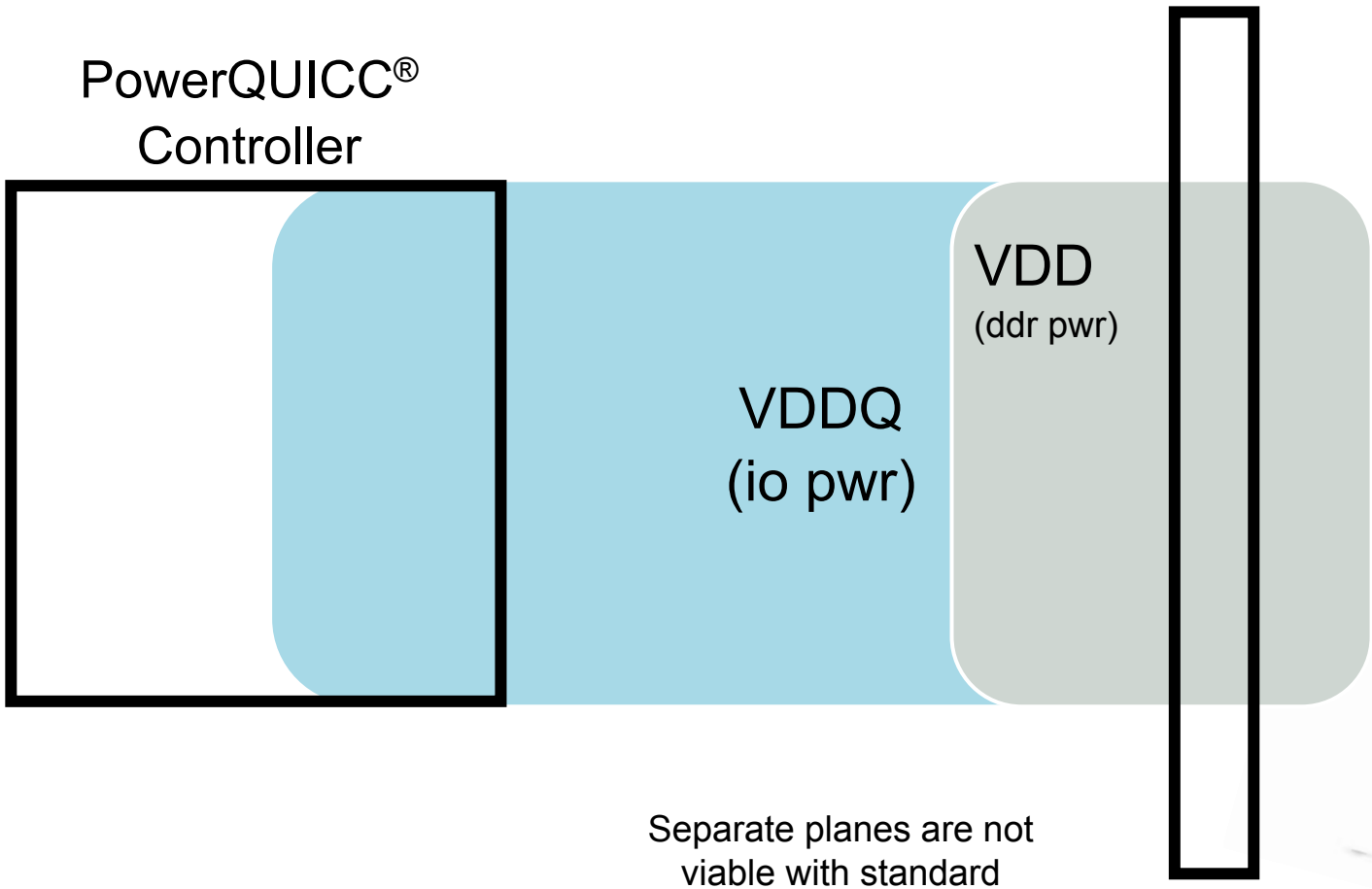
Pitfall 9 – Separate VDDQ/VDDIO



Separate planes are not viable with standard JEDEC DIMM memory modules

VDDQ and VDDIO are same plane on the modules

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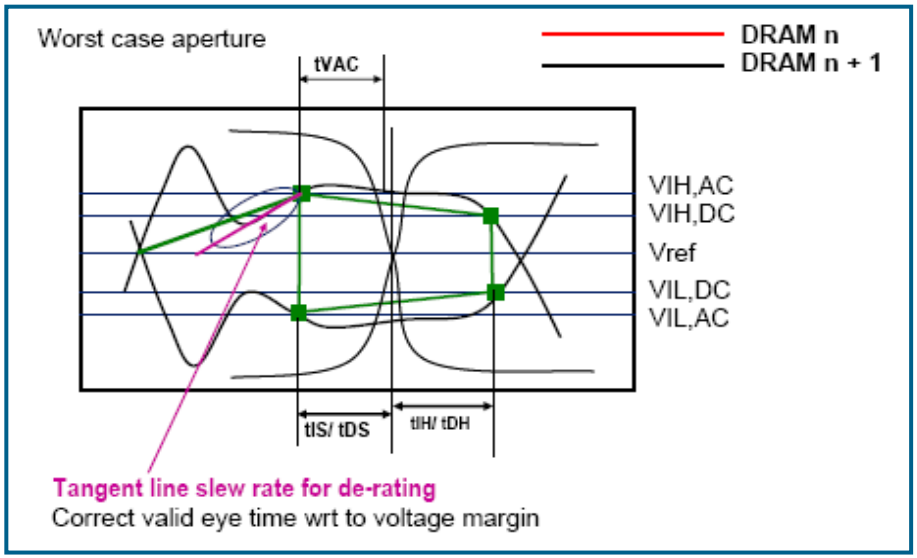
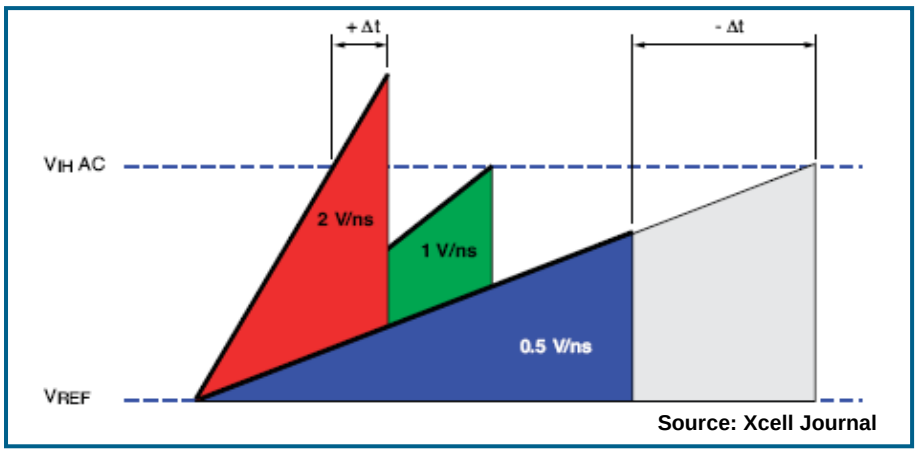
Pitfall 10– Slew Rate De-rating (Setup and Hold)





Source: Xcell Journal

Table 47 — Derating values for DDR2-667, DDR2-800

ΔtIS and ΔtIH Derating Values for DDR2-667, DDR2-800									
		CK,CK Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Command/Address Slew rate (V/ns)	4.0	+150	+94	+180	+124	+210	+154	ps	1
	3.5	+143	+89	+173	+119	+203	+149	ps	1
	3.0	+133	+83	+163	+113	+193	+143	ps	1
	2.5	+120	+75	+150	+105	+180	+135	ps	1
	2.0	+100	+45	+130	+75	+160	+105	ps	1
	1.5	+67	+21	+97	+51	+127	+81	ps	1
	1.0	0	0	+30	+30	+60	+60	ps	1
	0.9	-5	-14	+25	+16	+55	+46	ps	1
	0.8	-13	-31	+17	-1	+47	+29	ps	1
	0.7	-22	-54	+8	-24	+38	+6	ps	1
	0.6	-34	-83	-4	-53	+26	-23	ps	1
	0.5	-60	-125	-30	-95	0	-65	ps	1
	0.4	-100	-188	-70	-158	-40	-128	ps	1
	0.3	-168	-292	-138	-262	-108	-232	ps	1
	0.25	-200	-375	-170	-345	-140	-315	ps	1
	0.2	-325	-500	-295	-470	-265	-440	ps	1
	0.15	-517	-708	-487	-678	-457	-648	ps	1
	0.1	-1000	-1125	-970	-1095	-940	-1065	ps	1

Source: JEDEC 79-2C

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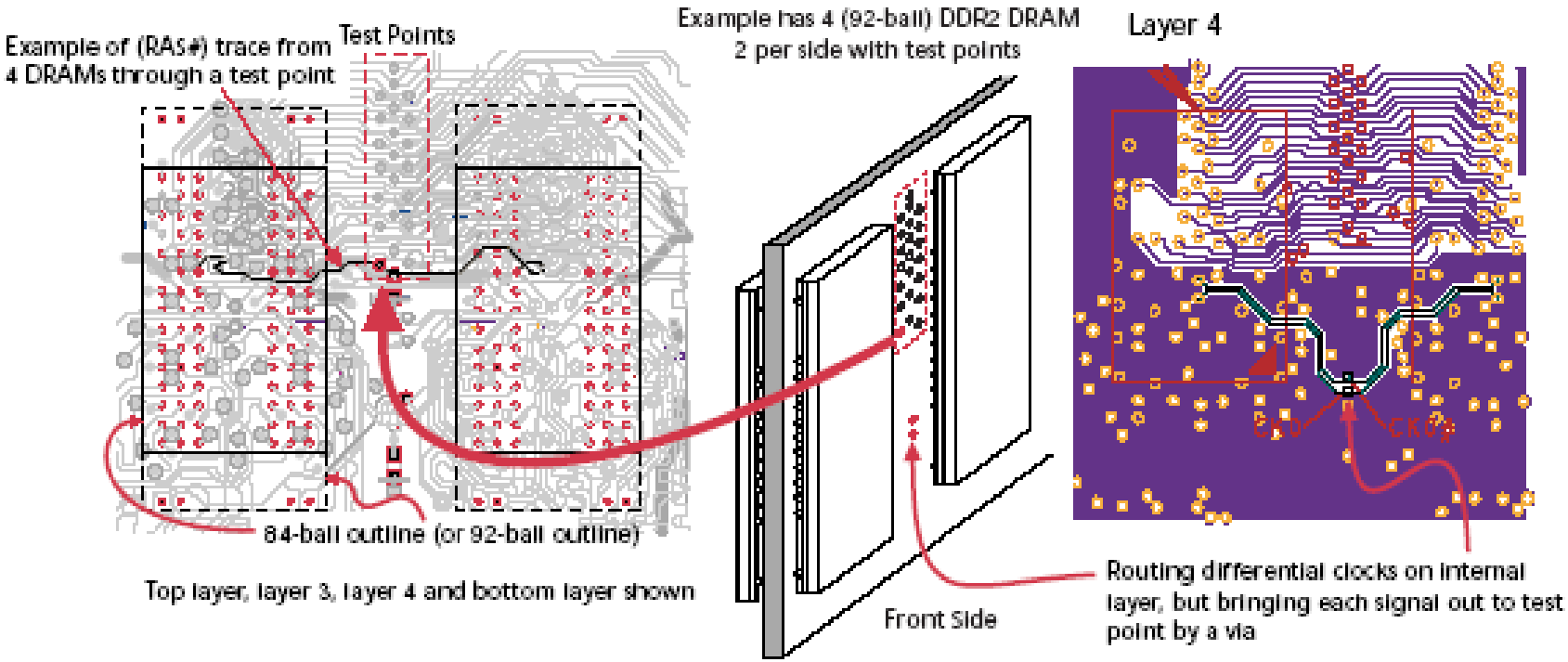
Pitfall 11 – No Debug or Testability on BGA Devices



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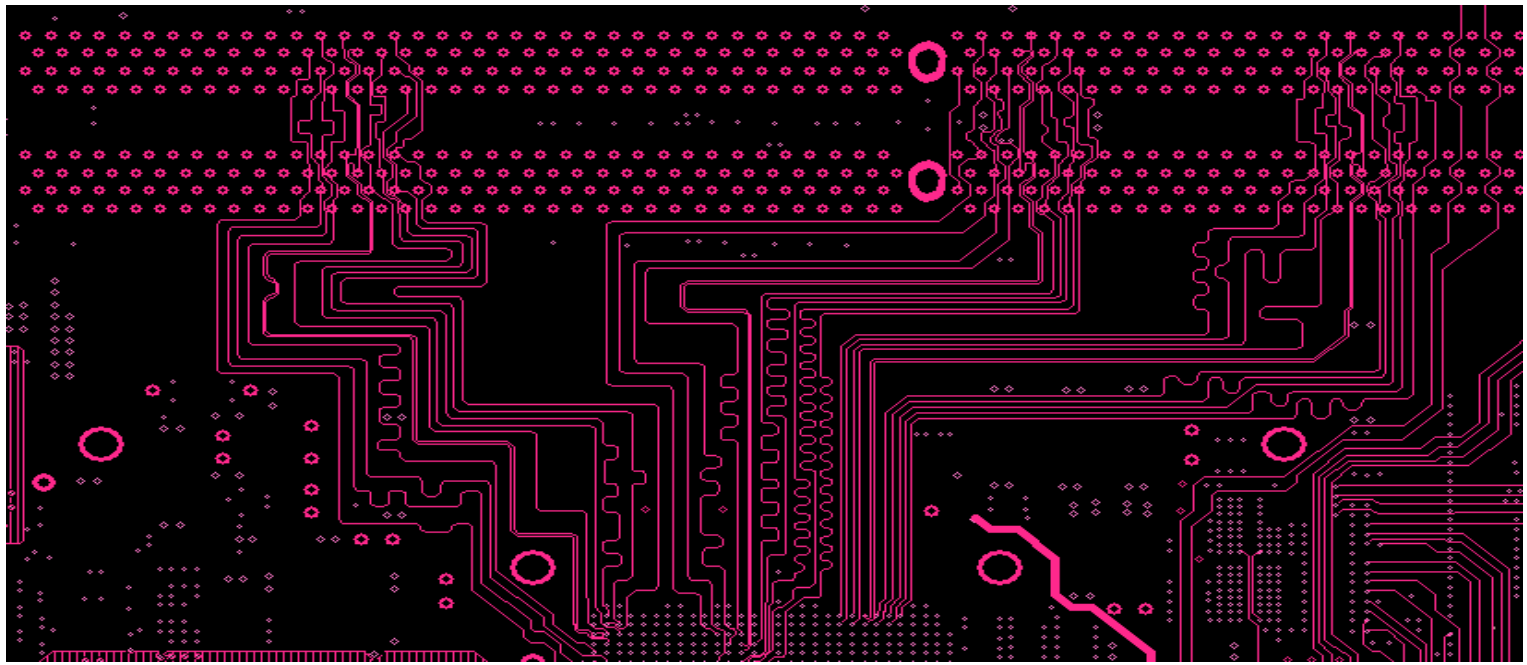
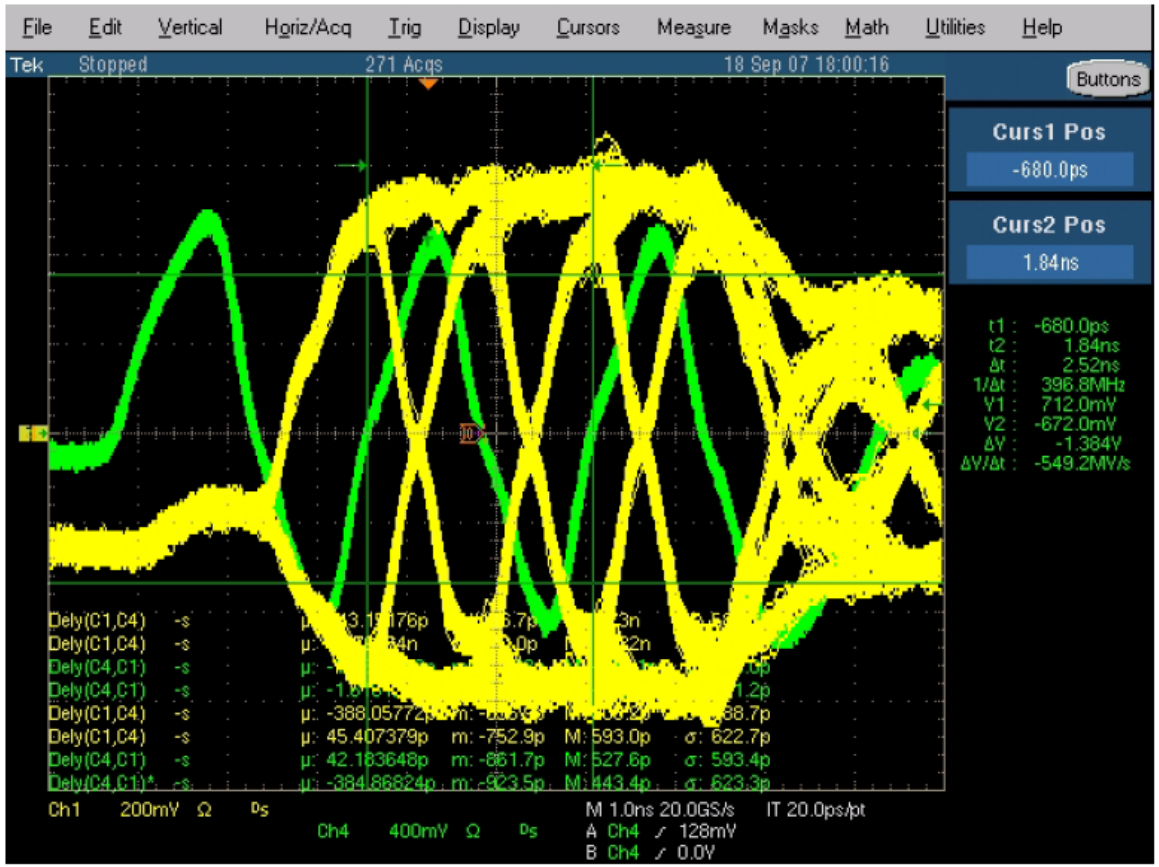
Layout Example – CTS8536

- Byte lane routing example



DDR3 - 800 MHz in the Lab

120 Ohm / Half Driver / 1 DIMM



Good margins across all data beats

Required
Tsu = 95 ps
Th = 170 ps

Measured Setup (Average)	646 ps	443 ps	440 ps	452 ps
Measured Hold (Average)	427 ps	405 ps	432 ps	850 ps

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Questions and Answers

Session Material

Session Location – Online Literature Library

http://www.freescale.com/webapp/sps/site/homepage.jsp?nodeId=052577903644CB

Demos

Pedestal ID	*Demo Title*

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